Link_A_Media Devices (LAMD) is the new leader in developing and manufacturing custom System-on-Chip (SOC) solutions for peripheral data storage devices, which include hard disk drives (HDDs) and solid-state-drives (SSDs). The SoC solution integrates the Read/Write Channel, disk controller functions, microprocessor(s) and memories, and servo processing for HDD application on a single chip.

Link_A_Media Devices provides the most leading-edge and advanced infrastructure and support for developing and manufacturing such SoC chips, including:

* Leading-edge CMOS process technologies
* State of the art cache memory technology
* Proven design flow and methodology
* Unmatched DFM flow and techniques
* High-speed/Low-power open microprocessor sub-systems
* New class of powerful data recovery methods
* IP blocks to support standard host interfaces
* Custom and semi-custom physical design
* Worldwide delivery logistics
* Unmatched DFM flow and techniques
* World-wide delivery logistics

With its unmatched data recovery technologies, Link_A_Media Devices’ custom SoC solutions deliver the highest areal densities, highest drive yields, and lowest power consumption. Those advantages enable hard disk drive (HDD) and solid-state drive (SSD) OEMs to continue to meet the growing demand for fast and low-cost data storage worldwide in consumer, computing, and storage networking applications.

**CAREER OPPORTUNITIES**

**Analog Design Engineer**

**Job Description:**

- Have strong timing and signal integrity background of DDR2/DDR3/Flash memory interface system.
- Have strong knowledge of transmission lines and low-power termination schemes.
- Capable of providing design guidelines to PCB layout and perform post route simulations for timing and signal quality.
- Hands on DDR2/3 IO and associated control circuitry design experience with design tools including HSPICE and Cadence Spectre and familiar with physical layout and post-layout simulation.
- Familiar with lab equipments such as oscilloscope.
- Excellent communication skills and ability to interface with other teams and customers in a dynamic start-up environment. Familiarity with IBIS model is a plus.

**Experience:**

- MSEE with 5+ years of experience in transistor level circuit design.
- Experience of modeling hi-speed I/Os, PCB interconnects, and package with respect to parameters such as jitter, reflection, crosstalk, SSN and ground/power bounce.

**Junior and Senior ASIC Design and Verification Engineers**

**Job description:** We are looking for: Junior and Senior Design Engineers in both design and verification to work on System-On-Chip (SoC) solutions.

The qualified design applicant would be responsible for all aspects of the design activities, including architecture definition, design specification, design low development, logic design and verification, DFT, synthesis and timing closure, test vector generation.

The qualified verification engineer would be involved in architectural modeling, reference model based verification, design reviews, test- planning, random test generation, debugging and coverage measurement. Familiarity with digital signal processing, SAS, SATA, PCIe is a plus.

**Junior ASIC / Digital Engineers:**

- 0 to 3 years experience and BSEE / MSEE or equiv., recent university grads with the appropriate background and experience will be considered.
Senior ASIC designers:
- with experiences in all aspects of RTL design flow from specification/architecture definition to design and verification.

Verification engineers:
- MS or BS with strong abilities in general purpose programming language (such as C++/C), scripting language (such as in Perl), HDL design and modeling language are required.
- Strong abilities in Experience with VLSI EDA tools - VCS, NCVerilog, Formality, DCT, RTL-compiler, PrimeTime etc., FPGA emulation is strongly desirable.

Staff engineers:
- must have hands-on experiences in all aspects of RTL design flow from specification/architecture definition to design and verification.
- Strong abilities in HDL design, modeling language, and a strong background in verification methodologies including random and coverage driven verification is a must.
- Experience with VLSI EDA tools, VCS, NCVerilog, Formality, DCT, RTL-compiler, PrimeTime etc., FPGA emulation, SAS, SATA and PCIe is strongly desirable.
- MS with 5 years or BS with 7 years in ASIC design is required.

Senior Staff engineers:
- Are expected to have hands-on experiences in all aspects of RTL design flow from specification/architecture definition to design and verification. Strong abilities in HDL design, modeling language, verification methodologies including random and coverage driven verification is a must.
- Experience with VLSI EDA tools, VCS, NCVerilog, Formality, DCT, RTL-compiler, PrimeTime etc., FPGA emulation, Knowledge of SAS, SATA and PCIe is strongly desirable.
- MSEE with 10+ years or PHD with 5+ years in ASIC design is required.

Jr. & Sr. Level Firmware/Software Engineers
Job description: Flash memory is a ubiquitous storage device used in all consumer electronics applications. NAND Flash memory has exceeded DRAM as not only the largest revenue but also fastest growing semiconductor segment. LAMD is uniquely positioned to develop and manufacture custom System-on-Chip (SOC) solutions for peripheral data storage devices, which include hard disk drives (HDDs) and Solid-State Drives (SSDs) based on NAND Flash. If you are a high energy computer professional and like to work in a challenging and rewarding environment with highly knowledgeable and innovative winning team, LAMD is the place for you.

Requirements:
- BS in either Computer Science or Electrical Engineering; MS is preferred
- Perform system integration, validation and debugging of FPGA and SoC design
- Develop new test software and utility tools to validate SSDs compatibility and reliability for target applications
- Setup the SATA storage test systems and prepare test scripts for SSD evaluation
- Perform failure analysis by using storage interface bus analyzer and digital scope, identifying the issues, duplicating the problems, and resolving the issues with corrective actions
- Proficient in structured firmware and software programming (C/C++, assembly, script languages)
- Hands-on experience in verification and trouble shooting in an embedded firmware application preferable with ARM based development tools
- Good working knowledge of design in digital logic, FPGA and SoC
- Experience of firmware debugging tools such as JTAG, In-Circuit Emulator, scopes and logic/bus analyzer
- Ability to work creatively and analytically in a problem-solving environment
- Good oral and written skills for communication and documentation
- Open to domestic and/or international travel for technical consultation

Jr. Level Requirements:
- Design, implement and evaluate real-time embedded system firmware for Serial ATA (SATA) and PCIe SSD controllers that optimize data access and cache performance, endurance and reliability for high performance desktop and enterprise class SSD products
- Work with major OEM customers to implement SSD functions per customer requirements, debug customer issues and prepare test report
- 6 month of development experience in team-based, complex programming in the embedded controller environment with Real Time Operating System (RTOS)
- Knowledge of mass storage systems: NAND flash memory, hard disk drives, SATA/ATA/PCIe, data caching and device drivers; Experience in the NAND flash storage device application and/or testing is a plus

**Sr. Level Requirements:**
- Design, implement and evaluate real-time embedded system firmware for Serial ATA (SATA) and Serial Attached SCSI (SAS) SSD controllers that will optimize performance, endurance and reliability for high performance desktop and enterprise class SSD products
- Work with major OEM customers to implement SATA SSD functions per customer requirements, debug customer issues and prepare test report
- 10+ years of development experience in team-based, complex programming in the embedded controller environment with Real Time Operating System (RTOS)
- 7+ years of firmware development experience in mass storage systems: solid state drives, hard disk drives, SATA/ATA storage devices, data caching or device drivers; Experience in the NAND flash storage device application and/or testing is a plus
- 5+ years of technical management experience
- A high level of skill in identifying performance critical algorithms for peripheral storage system optimization

FOR ADDITIONAL CAREER OPPORTUNITIES: www.link-a-media.com

*Physical Implementation Engineer  *SSD Architecture Staff Engineer  *Staff Systems Architect Engineer
*Staff Systems Design Engineer  *Senior Systems Validation Engineer