

Account Manager

LOCATION: Austin, Texas

Responsibilities:

This position is responsible for co-managing one or several product lines for one major customer including business and relationship. The detail activities include:

1. Demand Creation and Fulfillment, including demand forecast and order fulfillment.
2. Account calls and collaboration on technical / cost effective solutions to meet the client needs.
3. Developing relationships within the account at all levels.
4. Providing appropriate price quotes for responsible product and services then closes the sale. These services may be provided with the assistance of a technical support team.
5. Account team leadership for tactical business and technical issues.

Requirements:

BS, MS in engineering or science major with 5+ years experience in semiconductor industry. Familiar with semiconductor technology, design, process, and operations including test and product engineering. Strong customer orientation, excellent communication, and presentation skills are a must. Good English speaking skills and fluent in spoken Mandarin is a plus.

Strong ability to prioritize, organize and multi-task while working in a fast paced environment.

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Layout Engineer

LOCATION: San Jose, CA

Responsibilities:

Responsible for Memory (bit cell, pitch cell, IO & logic), Analog & Mixed signal layout. Plan Signals and Power buses. Hook up from leaf cell to top level.

Requirements:

AA or equivalent with a minimum of 8 years direct experience in hands-on layout methodology and tools such as Laker, Cadence, Caliber verification (DRC, LVS, Antenna...etc). Strong interpersonal and communication skills. Highly organized and detailed oriented.

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Sr. Engineers/Technical Managers

LOCATIONS: US or Taiwan

Responsibilities:

Chip implementation. eCPU implementation and sign-off. Provide on-site chip implementation support to TSMC major customers. Build up design methodology.

Requirements:

M.S. in EE or CS with 5-10 years experience in physical chip implementation. Proficient in advanced RTL-to-GDS design flow. Hand-on experiences with auto placement and routing tools. Deep understanding of the pros and cons of ASIC vs semi-custom design techniques/methodologies/flows. Familiar with TSMC 65nm and 40nm design rules. Must show proven record in production tapeouts of multi-million gate count large design. Possess design flow and utility program coding capability. Possess innovation at P&R design methodology. Customer oriented and willing to interface with customer and discuss specs. Willing to take tapeout pressure. Capable of working independently.

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Technical Marketing Manager

LOCATION: San Jose, CA

Responsibilities:

Support ARM-core based ecosystem and partners engagement.

Requirements:

MSEE and above with 5+ years of working experience with ARM or x86 processor. Experience in ARM microprocessor application, marketing and technical support.

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To apply for any of these positions, please send your resume to najobs@tsmc.com. Important: please specify the position and job location of the position that you are interested by listing it on the subject line of your email.