

2011 CASPA/SEMI High Tech Job Fair

JOBS AT INTEL

We are game changers, plain and simple.

At Intel, we see the everyday as a bar that continually needs to be raised. Step inside our world and you'll find one brilliant mind after another working together in a spirit of collaboration that is simply contagious.

Intel HIP Group Description:

Engineers in Intel's HIP (Hard IP) group design and develop multiple analog and high-speed I/O circuit blocks, including high speed serial IOs like PCI Express, USB, SATA, and DDR; and EBBs like PLLs, DACs, and other analog and high speed custom circuit blocks. The team designs on Intel's leading edge 22nm and 14nm technologies, and our designs are used across all ASDG (Atom and SoC Development Group) Platforms, including Handhelds, Tablets, Servers, Embedded Devices and Consumer Electronics. These products are key for Intel's SoC and Atom Everywhere Strategy. This will be the place to exercise your creativity and passion for Analog and Mixed Signal Design!

Intel HIP Sites:

We plan to hire multiple engineers in our two main sites: Folsom (outside of Sacramento, CA) and Chandler (outside of Phoenix, AZ). We have a few targeted positions available in Santa Clara, CA, and we are also looking to hire in our international sites of Penang, Malaysia and Bangalore, India. POSITIONS AVAILABLE IN THE INTEL HIP GROUP:

PLL Design Engineer:

Analog, Mixed-Signal, Design Engineer with skills and expertise in PLL design. The candidate will own various aspects of LC PLL design, including behavioral modeling, simulation, supervision of layout, post-layout simulations, RV/Agingsim, validation, and electrical verification of the circuits.

Qualifications required: Candidate must have an MS in EE, and several years of experience in analog or mixed-signal design and SOC design tools and flows. In addition, candidate must have: knowledge of high speed CMOS circuits, LC Phase lock loops (PLLs), and Clock circuits; ability to own all aspects of complex analog and mixed signal circuit blocks with minimal supervision; low power design knowledge; high speed I/O design knowledge including an understanding of the silicon design, signal integrity concepts, and power delivery fundamentals; good understanding of overall chip design flows; excellent communication,

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presentation and organizational skills; and hands-on design and silicon validation experience including oscilloscope and other lab equipment.

RCG Circuit design:

Responsible for delivering transistor level designs of IO interfaces and building block structures for Intel's 22nm/14nm process technologies. Use a top-down mixed-signal design methodology and Cadence CAD tools to complete project design cycles. The design tasks include CMOS transistor level circuit design and simulation to meet specifications, schematic and Verilog/RTL driven design entry, and schematic and layout synthesis. Responsibilities include defining innovative circuits, circuit simulation, timing analysis, cross-block functional validation, writing and validating Verilog-AMS behavioral analog models, the consideration of physical layout design and reliability issues, and testing/debugging circuits on silicon in the Design Validation (DV) lab. Qualifications include solid technical skills needed to design, simulate, layout, and debug High Speed IO designs, as well as innovative thinking and proven problem solving skills, the ability to organize and plan your work to meet program deadlines and write and present proposals and reports.

Minimum required: MSEE or exceptional BSEE with course work including analog transistor level circuit design and advanced VLSI design. Requires excellent knowledge of CMOS devices, high speed circuit design, low power techniques, clocking, signal integrity, silicon reliability, mixed signal design methodology and experience with SPICE Simulator and Transistor Level design tools.

Preferred (in addition to the minimum): PhD degree in Electrical Engineering; scripting knowledge in Perl/Tcl/Unix Shell; Verilog, Register Transistor Logic (RTL) design knowledge/experience; solid understanding of Synthesize/Auto Placement Routing (SYN/APR) concepts.

Experienced Circuit design:

Responsible for delivering transistor level designs of IO interfaces and building block structures for Intel's 22nm/14nm process technologies. Senior-level circuit design tasks include technology readiness and process definition, architectural definition of high-speed I/O and analog circuits, performance studies/simulations of critical analog circuit building blocks, and execution and development of the final Hard IP that will be delivered to our SoC

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customers. Qualifications include solid technical skills needed to design, simulate, layout, and debug High Speed IO designs as well as innovative thinking, problem solving, and leadership skills; the ability to independently organize and plan your work to meet program deadlines and write and present proposals and reports. Some roles may be expected to lead projects and supervise teams of junior engineers.

Minimum required: BSEE or MSEE with course work including analog transistor level circuit design and advanced VLSI design, plus 2-10 years design experience in high-speed I/O and analog circuit designs (various positions available for varying levels of experience). Requires excellent knowledge of CMOS devices, high speed circuit design, low power techniques, clocking, signal integrity, silicon reliability, mixed signal design methodology and experience with SPICE Simulator and Transistor Level design tools.

Preferred (in addition to the minimum): Strong analytical skills on system and/or architecture evaluation; in-depth knowledge of custom layout and reliability issues for high-speed precision circuits; knowledge of deep-submicron process rules, capabilities, constraints, and challenges; good understanding of industry trends and issues regarding high speed clocks and I/Os; and prior experience with the design of High Speed I/O > 5Gbps (Receiver, Transmitter, DLL, Clock Recovery, Jitter analysis, and Equalization schemes).

RCG RTL design/verification:

Responsible for the development of high speed serial IO digital logic for delivery to our System On Chip (SOC) customers. Use state of the art digital design tools and flows, and responsible for all stages of digital design, with a particular focus on microarchitecture, RTL design and coding, timing, overall reuse quality, RTL verification planning and execution, and testbench development. Qualifications include the ability to learn quickly and work effectively in a highly dynamic environment, as well as strong problem solving, good interpersonal communication and solid teamwork skills.

Minimum Required: BS in EE or CompE or equivalent with course work including digital design techniques, tools and flows familiarity; coding experience in Verilog or other high level logic modeling language; and RTL simulators working knowledge.

Preferred: (in addition to the minimum): MS in EE or CompE or equivalent with prior work/internship experience or course work knowledge including coding and debugging in System Verilog; basic understanding of coverage based verification; familiarity with high speed serial protocols such as PCI Express, SATA or USB; and digital design and verification experience through Co-ops or Internships.

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Experienced RTL design/verification:

RTL design engineers are responsible for interpreting the architecture spec and converting it to an implementable microarchitecture spec, coding the design in verilog, and participating in all aspects of the quality checks including clock crossing, lint checks, gate level simulations, and coverage reviews. In some cases the position will require working closely with the APR team to assure that timing goals are met. PreSilicon Verification Engineers are responsible for creating test and coverage plans to be used in the verification of complex Serial PHYs, analog and/or memory interfaces, and creating robust test environments using the following techniques/tools: System Verilog, Synopsys VCS Simulator, OVM methodology, and Assertion based coverage measurement. Qualifications include the ability to learn quickly and work effectively in a highly dynamic environment, as well as strong problem solving, good interpersonal communication and solid teamwork skills.

Minimum Required: BSEE or MSEE degree with coursework in digital design, Very Large Scale Integration (VLSI) design, computer architecture, IC development methodologies and Design-for-Test (DFT). Additional qualifications include: 2-10 years of VLSI Front-end and/or pre-silicon verification experience (multiple positions available for varying levels of experience); Register Transfer Level (RTL) development experience; programming and/or scripting (C++, Perl* and others) ability; and familiarity with flows and tools for VLSI logic design and/or functional verification .

Preferred: (in addition to the minimum):

Working experience on the DDR3 JEDEC protocol or complex serial PHY protocols (SAS, SATA, PCIE, USB3); and in-depth knowledge of System verilog and verification methodologies like OVM.

Structural (Backend) Design:

Responsible for taking RTL code through synthesis, place and route, static timing, etc. to produce DRC-clean GDS for integration with other blocks. Tasks include defining clock and other timing constraints, analyzing and fixing timing violations, clock tree synthesis, formal equivalence checking, and LVS/DRC analysis. Qualifications include the ability to learn quickly and work effectively in a highly dynamic environment, as well as strong problem solving, good interpersonal communication and solid leadership and teamwork skills.

Minimum Required: BSEE or higher with coursework in CMOS and VLSI design, timing analysis, and hierarchical design methodology. Some positions may require 2-10 years of

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structural design industry experience (positions available for varying levels of experience) including experience with Prime Time, Synopsys Synthesis and ICC based backend design, as well as tapeout and full chip timing.

Preferred: (in addition to the minimum):

Experience in handling of complex structural design partitions and logic that interfaces with high speed analog blocks. Scripting ability in Tcl or Perl.

Design Automation:

Responsible for EDA software design and methodology development, including the integration of new tools into existing SoC flows and customization of standard EDA flows as well as new tool evaluation studies, developing custom automation capabilities, and expert tool and flow support for the front end and back end design teams. Qualifications include familiarity with CMOS & VLSI circuit design and verification challenges and development flows, software development using Tcl and/or Perl, the ability to learn quickly and work effectively in a highly dynamic environment, as well as strong problem solving, good interpersonal communication and solid leadership and teamwork skills.

Minimum Required: BSEE or higher with coursework in CMOS & VLSI circuit design and verification. Some positions may require 2-10 years of design automation industry experience (multiple positions available for varying levels of experience) including experience with industry standard EDA tools/flows for analog, digital, and physical design as well as reliability verification and static timing analysis. Programming skills including scripting in Perl and Tcl, c-shell are required.

Preferred: (in addition to the minimum):

Experience with Synopsys and Cadence tools; familiarity with SOC models (RTL, LIB, LEF), VLSI design flow, and full chip integration flow.

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Join Intel Mobile Communications (IMC) Allentown, PA

Hardware Architect Concept Engineering (Req 594118, 3 opens)

General Requirements:

Positions are available in the Concept Engineering Hardware Architecture team that specifies the solutions for 2.5G/3G/HSPA/LTE handset baseband chips. Required: BS Degree, 7 years experience with of ARM/DSP based SoC architectures, bus architectures, and peripherals for mobile handset baseband device. Knowledge of power savings techniques, process technology, and system modeling preferred.

1. Software Architect Concept Engineering (Req 594120, 6 opens)

General Requirements:

Positions are available in the Concept Engineering Software Architecture team that specifies the Software Architecture for 2.5G/3G/HSPA/LTE handset platform solutions. Required: BS Degree, 8 years experience in a software architecture/development organization in the embedded software or mobile phone business, knowledge in C programming and object oriented techniques. Knowledge of system requirements definition, UML modeling, and HW/SW partitioning preferred.

Join Intel China

Intel China takes an active role in the development and evolution of the country's computing industry as it contains sales and marketing operations, design centers, technology labs, state-of-the-art manufacturing facilities and wafer fab in Beijing, Shenzhen, Shanghai, Chengdu and Dalian.

Beijing (Sales & Marketing Office)

1. Credit Manager, Beijing (Req 590560)

General Requirements: Work experience in Finance in a multinational environment or previous experience in Credit, banking, and /or insurance are an advantage.

Chengdu (Assembly & Test Plant)

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2. Assembly Process / Equipment Module Engineer (Please send CV to staffing.chengdu@intel.com)

3. Shift Manager (Please send CV to staffing.chengdu@intel.com)

4. Customs Strategic Program Manager (Req 591661)

General Requirements: For Assembly Engineer, a BSc or Master in Mechanical / Electrical Engineering, Automation, Chemical or Materials is required. For Shift Manager, an Associate, BSc or Master in Engineering with 3 years of supervisory experience. For Customs Manager, a degree in finance and/or legal discipline with hands-on experience in handling and solving custom issues in China.

Dalian (Wafer Fabrication Plant)

5. Duty Free Compliance Project Manager / Senior Analyst (Req 594528)

6. Financial Analyst (Req 587874)

7. Process Engineer (Req 591433)

General Requirements: For Duty Free Manager / Senior Analyst, a BA or MBA (preferred) in Business, Finance, Supply Chain Management or related discipline with 7+years of factory and/or supply chain work experience. For Financial Analyst, a BA or MBA with majors in Finance, Economics or Accounting. Candidates must have a firm grasp of financial statements and their interrelationships. For Process Engineer, a BS, Master or PhD in Engineering or Sciences with 3+ years of semiconductor industry experience.

Shanghai (R&D Center)

8. Senior Software Engineer (Please send CV to staffing.sh@intel.com)

9. Software Engineering Manager (Please send CV to staffing.sh@intel.com)

General Requirements: BSc or Master in Computer Engineering / Science or Electrical Engineering. For Engineer, hands-on proficiency in C and/or C++ programming languages and experience in software development and testing on Windows and/or Linux platform. For Manager, 8+ years of software development experience in embedded real-time, graphics, OS kernel, media frameworks, and/or systems.

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Join Intel India

Intel India is Intel's largest non-manufacturing site outside of the United States, focusing on creating innovative products that advance the next generation of technology. Our main areas of operation include software and hardware design and development. Reach us at intel_indiastaffing@intel.com

Research Scientist: Emerging applications, parallel programming, and multi core/many core architectures. Preference will be given to candidates with significant experience in parallel programming

DFx Micro Architect: ASIC front end design which includes Architecture, Micro-Architecture, RTL coding and validation Knowledge with basic Design for Test, Design for Debug and Design for Validation (DFx) techniques

Engineering Manager: Demonstrated ability to lead a software team developing advanced technologies using software best practices - Understanding of Windows* driver concepts, graphics related experience would be an added advantage familiarity with display and/or 3d and/or 2d and/or video technologies

Hardware Micro architect: Relevant ASIC design, validation and micro architecture development experience in front end processes including Register Transfer Level (RTL,) development, functional and performance verification. Expertise in micro architecture development, design and integration of design blocks (IP) to system-on-chip (SoC) components

GPU Performance Architect: The candidate should possess deep understanding of Graphics architecture, good knowledge of validation and debug flows in RTL, emulation and post silicon along with a high degree of Self Motivation and technical independence.

Software Architect: You should possess a Master of Technology from a reputed institution with more than twelve years of industry experience, demonstrated technical leadership and architecture development for any software product.

In addition to the above, we are also looking for both Experienced & Fresh Masters / PhD candidates in the below areas:

Front End Design / Validation Engineers Design Automation Engineers

Structural Design Engineers Graphics Validation Engineer

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Join the Intel Architecture Group – Malaysia

From data centers to desktops, laptops, netbooks, handhelds, embedded devices, and consumer electronics, Intel Architecture Group (IAG) Malaysia designs microprocessors, chipsets and system-on-a-chip (SOC) that have made all these state-of-the-art innovations possible.

Principal Engineer, Validation (Req 597220)

Staff/Senior Electrical Validation Engineers (Req 591886)

Staff/Senior Silicon Validation Engineers (Req 591887)

Staff/Senior Digital Design Engineers (Req 591241)

Staff/Senior CPU VLSI Design Engineers (Req 591243)

Staff/Senior CPU Pre-Silicon Design Validation Engineers (Req 591244)

Staff/Senior IO Mixed Signal Circuit Designers (Req 591249)

Staff/Senior Design Automation Engineers (Req 591250)

Principal/Staff/Senior System Validation Engineers (Req 591251)

Staff/Senior Product Development Engineers (Req 591253)

Senior SoC Design Engineer (Req 591764)

General Requirements:

BSc, MSc or PhD in Electronic/Computer Engineering with minimum 5 years' relevant working experience for Senior positions and 7 years' for Staff/Principal positions. Multiple vacancies are available for each position.

Join the Finance Group - Malaysia

Intel Malaysia Finance welcomes you to Penang and Kulim for a successful career in Finance and Accountancy! It is the largest Intel finance organization out of the United States with approximately 270 employees located in Penang and Kulim. The organization consists of 5 major functions: Operations Finance, Finance Shared Services Center, Global Tax & Trade, Internal Audit and Treasury.

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12. Finance Analyst/Accountant (Req 585783)

13. Finance Analyst/Accountant (MBA) (Req 585784)

14. Finance Intern (Req 585785)

General Requirements :

A Bachelor's degree in Accounting, Finance (or Business Administration majoring in Finance), Economics, or an equivalent, with a GPA of 3.0+. You should also be proficient in Microsoft Excel, Word and PowerPoint. Multiple vacancies are available for each position. Malaysian citizenship or the ability to secure the appropriate work permit is required.

Join Intel Vietnam

Intel takes a giant leap into Vietnam by investing US\$1 billion to build a semiconductor assembly and test facility in Ho Chi Minh City. This Vietnam facility is the seventh assembly site of Intel's global network. It also represents the first such investment by the semiconductor industry in Vietnam and is projected to eventually

employ about 4000 people. Scheduled to be the largest computer equipment and manufacturing plant in Vietnam, and the largest assembly test manufacturing plant Intel.

1. Manufacturing Supervisor (Req 586772)

2. Shift Manager (Req 592910)

3. Industrial Engineer (Req 594191)

4. Failure Analysis Engineer (Req 594207)

General Requirements :

A Bachelor's degree in Engineering (Industrial, Mechanical, Electrical and Material), Applied Physics, Chemistry, Management Science or Mathematics. Minimum 2 years of relevant experienced is required for Failure Analysis Engineer and Manufacturing Supervisor and 6 years for Shift Manager. You should also be proficient in both Vietnamese and English.

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Join Intel Asia Pacific

1. APAC Sales and Marketing Rotation Program (Req 585035)

General Requirements:

Recent graduates with bachelor degree in Electronics Engineering or Computer Science and M.B.A. Specific plan and objectives to return to your home country in APAC(Target Country: Taiwan, Indonesia, Malaysia, Vietnam) to work and develop your career with Intel. Permanent right to work in the country you will be finally placed. Prior 2 to 3 years of working experiences in MNC companies. Strong communication and presentation skills, demonstrated leadership abilities, and a record of extracurricular activities above and beyond standard university requirements would be an added advantage. Knowledgeable in Microsoft* Office* programs

2. Finance Analyst (Req 597028, Req587865) – Hong Kong

General Requirements:

BA/ B.Sc./ MA/ M.Sc required. Professional accountancy qualification (ACA, ACCA, CIMA) desirable. Previous experience in an analytical role - minimum of 1 year. Requires good attention to detail with the ability to analyze data, solve problems and identify and communicate trends.

Having the ability to deal with large quantities of information and opinion and be able to extract key data items is also a key requirement. Requires the ability to deal comfortably with senior management, influencing and reinforcing the finance agenda. Hong Kong citizenship is required.

MDG/CCDO

Layout Design Automation (DA) Engineer: Hillsboro, OR (Req #587750)

Requirements: Bachelor of Science in Electrical Engineering or computer Science with 3+ years experience - Good fundamental understanding of layout concepts and methods and CAD tools. - Programming aptitude, good debug skills, and experience with Tcl, Perl, and design environment

Mixed Signal Validation Engineer: Hillsboro, OR (Req #596380)

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Requirements: BS or MS degree in Electrical or Computer Engineering. Bachelor's 5+ years of experience and Master's candidates should have 3+ years of experience in hardware validation -Excellent understanding of basic analog, mixed signal circuits -Familiarity with high speed I/O design, knowledge of signal integrity issues -Experience with circuit simulation tools like Pspice and application of circuit analysis concepts -Experience in digital logic design and simulation using Verilog/VHDL -Hands on experience with UNIX* or Linux* -Strong debugging skills -Ability to read and interpret technical specs and Register Transfer Level (RTL) code - Ability to lead a small team, including requirement gathering, goal setting, progress tracking, and executing to objectives.

MDG/SDG

Pre-Si Verification Engineer: Santa Clara, CA (Req# 591696)

Requirements: Master of Science degree in Electrical Engineering and/or Computer Engineering and/or Computer Science with 4 years of related experience - Strong understanding of computer architecture and micro-architecture design concepts - Mixed signal validation experience for high-speed circuits - Good understanding and interest in working on analog/digital boundary and understanding of analog design - Experience working with simulators such as Mynx, cadence-AMS or nanosim - Experience in developing checkers, monitors, test generators - Experience in using modeling languages Specman, System Verilog

Logic Design Automation Engineer: Santa Clara, CA (Req# 592365)

Requirements: BS or MS in Computer Science, Electrical or Computer Engineering with 5+years or 3+years respectively in design automation experience in front end logic design or validation automation -Expert coder with Perl, Verilog, C shell and Shell Scripts -Experience with Specman and VCS -Experience with System Verilog

-Experience with TCL, C or C++

Architectural Validation Engineer: Fort Collins, CO (Req# 593744)

Requirements:

BS or MS degree in Electrical/Computer Engineering or Computer Science, with at least 2 years of industry experience - Strong programming skills in C++ and Perl - Experience with Verilog simulation - Experience with processor architecture and micro-architecture

Senior Design Engineer: Santa Clara, CA (Req#593969)

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Requirements:

BS (with 5+ years of experience) or MS (with 2+ years of experience) in Electrical Engineering, Computer Science or Computer Engineering - Experience in Circuit Design and Verification - Experience in Synthesis Place and Route (P&R) tools and methods - Experience in Timing Analysis

DFT (RTL) Engineer: Santa Clara, CA (Req # 594536)

Requirements: BS (with 4+ years experience) or MS (with 2+years experience) in EE, CE or CS

Requirements:

-Experience in advanced DFT architecture and micro-architecture design concepts

Pre Si Verification Engineer: Santa Clara, CA (Req# 594537)

Requirements: BS (with 4+ years experience) or MS (with 2+ years experience) EE, CE or CS - Strong understanding of CPU architecture, computer architecture and micro-architecture design concepts - Programming experience with high level programming languages (example C, C++) - Scripting languages (example Perl, shell*, PHP*) - Hardware description languages (Verilog*) - Experience with microarchitecture verification

Power Management RTL Engineer: Santa Clara, CA (Req#594539)

Requirements: BS (with 4+ years experience) or MS(with 2+years experience) in EE, CE or CS -Experience with advanced computer architecture and micro-architecture design concepts -Experience with Power control unit or power management protocols. -Experience with Processor design

RTL/AV Design Automation Engineer: Santa Clara, CA (Req#595666)

Requirements: BS (with 4+ years experience or MS (with 2+ years experience) in EE, CS or CE -Experience in simulation tools and environments -Experience in gate level simulation and verification -Experience programming in C shell, PERL or UNIX -Experience System Verilog

Front End RTL Engineer: Santa Clara, CA (Req#595669)

Requirements:

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BS (with 4+ years experience) or MS (with 2+ years experience) in EE, CE or CS -
Experience in advanced computer architecture and micro-architecture design concepts -
Experience in Processor Design

Analog Design Engineer: Santa Clara, CA (Req#595758)

Requirements:

BS in EE, CE or CS with 4+years of experience or MS in EE, CE or CS with 2+ years
experience - Experience with Analog IC design encompassing circuit design, circuit
simulation, and physical layout . - Experience with analog blocks such as ADC, DAC, filters,
Power Amplifier

-Experience with Temperature Sensor, Voltage Regulator, Bandgap, or Operational Amplifier

Microprocessor Design Engineer: Hudson, MA (Req#597979)

Requirements:

BS in Electrical Engineering, Computer Engineering, or Computer Science with 6+ years of
experience or a MS in Electrical Engineering, Computer Engineering, or Computer Science
with 4+ years of experience in the following: -Strong background in Computer Architecture,
Digital Logic Design, Logic Simulation, and Software Development -Working knowledge of
Unix* and Windows* -Strong hardware debug skills

Job Title: Electrical engineer

Working Location: Chengdu

Responsibilities:

Lead the electric system sustaining for site power support, include operation & maintenance support to substation, transformer, generator, UPS(Uninterrupted Power Supply), life safety system, bus bar, VFD(Vary Frequency Device), and all electric cable & panels. Contribute to new project through design, equipment shake down, construction quality assurance, test & commissioning and final hand over. Leverage the electric mastery to operation team.

Qualification:

Bachelor degree or above on electric or power related.

Be able to speak fluent English.

SHANGHAI Position

Position: Application Engineer / Sr. Application Engineer

Function: Low Level Driver

Work location: Shanghai, PRC

Job Descriptions:

- General knowledge of embedded systems
- Familiar with basic SW and HW Architecture of mobile phone system- Hands-on experience with Low Level Driver development (one or several of the following Driver modules: Audio, LCD, UART, SIM card, Charger, Power Management, Accessory, Backlight/Keypad, USB, IrDA, IIC, RF Drivers)
- RTOS experience (Nucleus or OSE preferred)
- Familiar with real-time debugging tools, e.g. Lauterbach trace32- Familiar with test and development equipment such as CMU200, Logical Analyzer, Oscilloscope

Qualifications:

- Good teamwork and communication skills
- Willingness to both domestic and overseas travel
- Fluent English is a must
- 2.5G / 3G protocols knowledge is a plus

Position: Application Engineer / Sr. Application Engineer Function: Protocol Stack

Work location: Shanghai, PRC

Job Description:

- General knowledge of ARM architecture and embedded systems
- Good knowledge in SW and HW structure of mobile phone system
- Experience on real-time debugging tools such as Lauterbach trace32
- Hands-on experience with 2G/3G protocol stack development and problem resolving
- Experience like in TCP/IP,PPP,ATC,NAS,and GAS is preferred
- Familiar with test and development equipment such as CMU200, Logical Analyzer, Oscilloscope

Position: Application Framework Architect

Work location: Shanghai, PRC

Job Description:

- To drive and contribute to architecture activities for Open OS Based Application Framework platforms especially Android Framework
- To mentor development team on design, implementation & optimization concepts for OOS Based Application SW
- To execute prototyping activities for concept verification
- Excellent demonstrated experience in at least two of the following areas:
 - Linux/Android System Optimisation
 - Graphics and UI (With excellent understanding of Android 2D and 3D requirements)
 - Multimedia (Audio and Video)
- Excellent understanding of Android framework architecture and app development concept on top
- Excellent understanding of Android SDK for applications
- Excellent understanding of Embedded Linux middleware applications (Logging, IPC, etc)

Qualifications:

At least 8 years of experience in the embedded and wireless domain. In addition, the following skills are mandatory:

At least 5 years of hands-on experience in a Linux Based platform

At least 1 year of hands-on Android based experience

Position: Application Engineer/ Sr. Application Engineer

Function: MMI**Work location: Shanghai, PRC****Job Description:**

- Design and develop reference for Intel Mobile Communication mobile phone solution. The Reference MMI software provides full-functional graphic man-machine-interface features including framework development, protocol related applications, multimedia application and 3rd party integration, which run on IMC entry level mobile phone and services as reference package for IMC customers.
- Cooperate and co-work together with IMC global customer for mobile phone MMI software development and customization, based on customer production.

Qualification:

- Solid programming and debugging knowledge with C language in embedded software development environment
- Good experience and understanding on software design, development, release and maintenance processes
- Good understanding on GSM mobile phone software architecture and concepts, with solid knowledge based on MMI related GSM specifications
- Bachelor or Master degree in Communication, EE or related areas
- Good knowledge on the system debugging and integration-

Position: Application Engineer/ Sr. Application Engineer**Function: Integration****Work location: Shanghai, PRC****Job Description:**

- GSM/GPRS mobile phone software integration and configuration management
- Responsible for software release management and software integration
- Training to internal and external customers may be required
- Tool development and maintenance
- Good programming skills
- Good understanding of Mobile Phone features and system know-how
- Knowledge on ClearCase software and Perl language programming is an advantage

BEIJING Position

Position: TD-LTE Software Engineer

Function Area: System/Lay 1/Protocol Stack/Algorithm;

Job Responsibility:

- Work with L1/Protocol/driver/IC team, to define the system flowchart, debug the issues in system level, review the whole LTE system design, review the algorithm efficiency and HW/IC implementation efficiency;
- Focus on TDD LTE Protocol (L2/L3)/physical layer design, program, debugging and development. Also will work with HW/IC team and driver team to ensure the system will run smoothly, need work with test team to develop the test case, do field test and debug the issue found during testing;

Position: TD-LTE Hardware Engineer

Function Area: Baseband/RF;

Job Responsibility:

- Will work with IC team to do reference design, work with Driver team to ensure the HW system design can fulfill the SW requirement, work with our vendors for all kinds of peripherals design/debug and integration, ensure platform RF performance can fulfill the certification with good margin.

Position: TD-LTE Engineer

Function Area: FPGA/IC verification;

Job Responsibility:

- Will co-work with IC design team to verify the algorithm on FPGA board, IC bugs debugging, new algorithm verification, repeat the system test and field testing issues and fix, debug the issue on FPGA board together with Protocol/L1/Driver team in Labs and field;

Position: System Architect

Function Area: Concept Engineering of Audio/MM/Platform HW Architecture/Security/tools

Job Responsibility:

- Define, concept and develop platform solutions for Mobile Terminal solutions focusing on 2-2.5G & TD-LTE modem functionality (bearer), Voice, Music and Video applications, together with best in class system costs, audio and video quality, power consumption and scalability;

- Technically very proficient individual contributor role and able to work independently to solve issues, and also can be effective in leading a global team to achieve biz goals;

Position: Project Manager

Function Area: Software, System Integration/Release/Build/ System SW & Tools

Job Responsibility:

- Overall responsibility for the project execution: planning of project schedule, budget and resource demand, execute the project within granted project boundary (time & cost), tracking and reporting of project status on a regular basis;
- Leads the team in Milestone reviews both internal and external, project risk management, managing Customer Communication and Status reporting;
- Coordinates with function groups from Hardware, Software, verification, concept engineering, etc to staff the project team worldwide;

Position: Sr. Application Engineer

Function Area: Software, Low Level Driver/System Debugging

Job Responsibility:

- Design and develop systems solution making specific determinations about system performance, come out new platform solution with global team together;
- Review and input to the core function code change;
- Expected to conduct analysis and development on system level;
- Responsible for developing SW solution to demonstrate the new proposal;
- Working closely with Software Project management team, Software release team, Verification team and other component team, provide recommendations to management concerning issues of programmer productivity and software development management;

Position: Sr. Application Engineer

Function Area: Software, Protocol Stack Analysis/Protocol Stack Testing

Job Responsibility:

- Responsible for SW Development of Protocol Stack on the mobile phone product, mostly focus on Adaption Module between PS and application layer;
- Responsible for new requirement analysis, overall design, coding, unit test/inspection, etc, through the SW lifecycle to make sure the quality of SW delivery;
- Responsible for Critical issue debugging mostly on Protocol Stack Adapter Module, research on the new technology on the PS area and provide inputs with the focus on log analysis from Protocol Stack view to the management.

XIAN Position

英特尔移动通信技术（西安）有限公司位于西安高新技术产业开发区。2005 年公司通过了由 DNV 颁发的 ISO 9001:2000 认证和 ISO/TS 16949 认证。现英特尔移动通信技术（西安）有限公司已成功开发出国内首款 40 纳米 CMOS 工艺低功耗手机芯片，该芯片支持 3GPP R7、EDGE 和 2G 通讯协议，并可通过外部接口支持 LTE 协议，同时具有强大的语音处理功能，还支持 USB HSIC 和 MIPI HSI 高速外部接口，多项技术在全球范围内皆处业界领先水平。

英特尔移动通信技术（西安）有限公司，将继续发挥其战略优势，提供高质量的集成电路设计服务，充分利用中国西部研发人才优势，满足中国本地客户不断扩大的需求，成为一个能够提供全套解决方案的全方位 IC 供应商，在半导体产业中再创佳绩。

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Job Profile List:

1. HWA (HW architecture) Concept Engineer **Urgent!!!**
2. HWA (HW architecture) Concept Engineering Manager **Urgent!!!**
3. MOD (Modem) L1P Concept Engineer for TD-SCDMA **Urgent!!!**
4. MOD (Modem) Concept Engineer for FW Architect TD-SCDMA/ TD-LTE **Urgent!!!**
5. MOD (Modem) Concept Engineer for DSP FW Architect 2G **Urgent!!!**
6. Platform Concept Engineer **Urgent!!!**
7. Platform Concept Engineer (Feature Requirement Management) **Urgent!!!**
8. Logic Physical Synthesis Engineer **Urgent!!!**
9. TD-LTE FW Development & Verification Engineer **Urgent!!**

1. HWA (HW architecture) Concept Engineer **Urgent!!!**

Job Description:

As a member of Concept Engineering Hardware Architecture team that specifies the solutions for 2.5G and 3G handset baseband chips, the candidate will be responsible for the Digital Baseband portion of the solution. This includes the overall HW architecture meeting the functionality and performance specified by the System Requirements. The candidate would be responsible for generating the Sub-

System Requirements, allocating the system requirements to the different baseband subsystems of the solution and specifying the implementation architecture to meet the requirements. The responsibilities of the Hardware Architect include some or all of the following:

- Definition of Digital Baseband HW architecture
 - Deep understanding of ARM/DSP based SoC architectures, bus architectures, peripherals, and security features.
 - Ability to design, implement, and simulate system models for architecture trade-off and bandwidth analysis
- Understanding of power savings techniques, technology, and algorithms
 - Ability to review and analyze process technologies and process options in support of low power design
 - Understanding of low power IC design architectures and system design architectures.
- Understanding of GSM/GPRS/UMTS Handset systems
 - Digital baseband HW architectures and interfaces
 - Analog baseband HW architectures and interfaces
 - Power management IC HW architectures and interfaces
 - Radio/RF HW architectures and interfaces
 - Knowledge of external component functionality and interfaces: memory, display, camera, external memory cards, connectivity (USB, BT, etc.)
- Understanding of IC design process and designs
 - Process technologies, standard cell libraries, memories, PLL's, clock generation, I/O buffers-
 - IC design, simulation, and testing methodologies
- Comprehend and communicate competitor Digital Baseband architectures and capabilities.
- Develop System Functional specifications that will be used to guide the Development organizations during product development.
- Generate system level requirements for the Digital Baseband portion of a product based on Marketing Requirements Document and industry norms.

Requirements:

- Ph.D or Master Degree on Electronics Engineering/Communication/ Microelectronics or relevant
- Minimum 7 years Engineering experience, 10 years Engineering experience will be preferred
- Experience with ARM based SoC architecture solutions
- Excellent communicator
- Must be able to work with people in many different cultures and in off-site locations
- Excellent team player
- Quick learner
- Able to deliver quality products on schedule
- Willing to work within a sensible development process framework
- Committed to documenting the development work
- The following skills and Experiences will be preferred:
 - Proven experimental skills and lab/bench expertise
 - Experience with system feature requirements development and management
 - Experience with DSP and/or ARM embedded processor development.

- Experience with 3GPP Standard
- Experience with the SW and/or HW development of Communication systems
- Experience with low power design
- Experience with system modeling tools

2. HWA (HW architecture) Concept Engineering Manager Urgent!!!

Job Description:

Build up and lead a world class hardware architecture team as a subgroup of the world wide HWA department to maintain leading edge hardware architecture/solutions for mobile terminals

- Develops the team to cope with current and future challenges for baseband chip hardware architecture
- Develops effective relationships with customers, contractors, clients, universities and partners.
- Responsible for proposing, developing and implementing leading edge architectural and IPR solutions for mobile terminal baseband/hardware projects and products
- Responsible for the development and continuous improvement of tools and methodologies relate to the HWA deliverables
- Handles all aspects of team's performance management.
- Staffing, recruitment and integration of new employees
- Teambuilding, coaching, conflict management and fostering Infineon's values
- Interfaces with the Component Development team, program management, and project management to resolve technical issues, to allocate resources to projects and to satisfy customer needs.
- Responsible for project planning for HWA team activities, as well as on time and within scope HWA deliverables to projects
- Applies lessons learned from current customer/platform issues to enhance future HW architectures, as well as influencing HW/SW partitioning
- Serves as communication link between his team and management in order to cascade goals and strategy downwards and to surface issues upwards.
- Supports marketing and sales in discussions with customers, partners and operators
- Full responsibility for functional budget to include but not limited to; functional HC, expense, capital equipment, T&L and training
- Leads a team of 5-10 hardware architect Engineers

Requirements:

- Ph.D or Masters degree of communication engineering or related field
- Minimum 7 years experience as functional manager in a Integrated Circuit company
- Minimum 8 years experience in a hardware architecture/development organization in the baseband mobile phone business
- Efficient, cost-effective team with rich blend of key competencies

- Highly motivated, high performance team which attracts high caliber concept engineers from other companies
- Continuous improvement of hardware architecture (cost, performance, functionality)
- Reduction of customization costs by ensuring high re-use of existing HW IP
- Excellent Communication with Project Managers, Program Managers, and the other development organizations
- Performance management including 100% of objectives set for all employees; full compliance with spirit and intent of STEPs process
- Achievement of personal and team objectives; focus on “what” and “how”
- Fluent in spoken and written English

3. MOD (Modem) L1P Concept Engineer for TD-SCDMA Urgent!!!

Job Description:

- Perform Research in the area of wireless communication mainly focusing on TD-SCDMA L1, EDGE evolution, 3G, 4G and LTE
- Take responsibility for defining detailed implementation specification based on feature requirement for implementation team
- Take responsibility for software and hardware partition for wireless transceiver
- Take responsibility for defining detailed implementation specification of algorithm for wireless transceiver
- Take responsibility for defining hardware interfaces and system resources according to performance requirements
- Modeling and Simulation of Signal Processing Blocks
- Modeling and Simulation of bandwidth and performance requirements
- System level modeling and reference data generation for verification
- Take responsibility for verification objective review
- Take responsibility for defining use case of block
- Tracking and participating in standardization process

Requirements:

- Ph.D or Master Degree Electronics Engineering/signal processing/wireless Communication/telecommunication or relevant.
- Good knowledge of wireless communication system standard, prefer experience in TD-SCDMA
- Good knowledge of digital signal processing
- Good understanding of modulation and demodulation algorithms for wireless communication
- Good communication skill and good team work
- Good knowledge of MATLAB, CoCentric and SystemC is preferred
- Experienced in VHDL /Verilog coding is preferred.

4. MOD (Modem) Concept Engineer for FW Architect TD-SCDMA/ TD-LTE Urgent!!!

Job Description:

Definition and design of Layer 1 Firmware for the TD-SCDMA/TD-LTE wireless standard.

- Architecture definition for TD-SCDMA/TD-LTE firmware
 - Mapping of TD-SCDMA/TD-LTE features and standard requirements to FW and algorithm requirements
 - Breakdown of requirements into FW components
 - Identify all relevant FW aspects for the TD-SCDMA/TD-LTE standard
 - Define scheduling and task priorities of FW components with respect to given real-time constraints and system resources (MIPS, memory) in a TD-SCDMA/TD-LTE system
- Concepts for partitioning between HW and FW (HW/FW split) in a TD-SCDMA system
- Verification concepts for TD-SCDMA/TD-LTE FW on block and system level
- Planning and selection of scheduling software
- Provide guidelines for implementation aspects of modem algorithms in a TD-SCDMA/TD-LTE system
- Customer interface for TD-SCDMA/TD-LTE FW related topics

Requirements:

- Ph.D or Master degree in Electrical Engineering with focus on Communications Engineering
- Expert knowledge in Digital Signal Processing and Communications Engineering
- Proven experience in implementing DSP FW for 3GPP Standards like TD-SCDMA/TD-LTE or UMTS
- Experience in SW/FW design for embedded real-time systems
- Fluent in spoken and written English

5. MOD (Modem) Concept Engineer for DSP FW Architect 2G Urgent!!!

Job Description:

Definition and design of DSP Firmware for 2G (GSM, GPRS, EDGE, EDGE Evolution) wireless baseband applications.

- Architecture definition for 2G DSP firmware
 - Mapping of given 2G features and algorithms to DSP FW requirements
 - Breakdown of requirements into FW components
 - Identify all relevant FW aspects in a 2G wireless system
 - Define scheduling and task priorities of FW components with respect to given real-time constraints and system resources (MIPS, memory) in a 2G system
- Concepts for partitioning between HW and FW (HW/FW split)
- Interface definition of HW accelerator blocks for selected DSP tasks
- Planning and selection of scheduling software for real-time operation in a 2G system
- Verification concepts for DSP FW on block and system level

- Provide guidelines for implementation aspects of modem algorithms (how can this algorithm be implemented)
- Support definition and design of HW accelerator blocks for selected DSP tasks

Requirements:

- Ph.D or master degree in Electrical Engineering with focus on Communications Engineering
- Expert knowledge in Digital Signal Processing and Communications Engineering
- Proven experience in implementing DSP FW for 3GPP Standards like GSM or UMTS
- Experience in SW/FW design for embedded real-time systems
- Good knowledge on optimised implementations of DSP algorithms
- Fluent in spoken and written English

6. Platform Concept Engineer Urgent!!!

Job Description:

- Responsible for quality and completeness of customer and system requirements for mobile phone platforms and components. About 2 projects in parallel with 1000 - 2000 requirements each depending on project scope.
- Participation in continuous improvement activities for requirements management and engineering.
- Product Requirements Management
 - Overall responsibility for Requirements Repository and documents
 - Gathering and elicitation of requirements/ needs from stakeholders
 - Requirements interface between the development team and internal and external customers/ stakeholders
 - Supports mapping of requirements to components
 - Monitors and tracks: quality of requirements and traceability
 - Drives requirement reviews
 - Requirements change handling/ participation in CCBs
 - Answers request for information together with sales, marketing and technical experts.
- Participation in continuous improvement activities
 - Alignment across chip and platforms projects in regular meetings
 - Provide customer requirements for reuse
 - Participate in continuous process and methodology improvement (TEC RE)
- Be internal and external interfaces operate on an international basis.
 - Internal: Business Line Marketing and System / Concept Engineering, Verification Management, Project and Program Management, Quality Management.
 - External: IFX customers.

Requirements:

- Ph.D or Master Degree on Electronics Engineering/Communication/ Microelectronics or relevant

- Professional experience in System Engineering or related disciplines
- Fluent in English
- Good expertise in Requirements Management
- Rational Requisite Pro
- MS Office (desirable including VBA)
- Adobe Framemaker (desirable)
- Social and communicative skills
- Self-organization

7. Platform Concept Engineer (Feature Requirement Management)

Job Description:

- Responsible for quality and completeness of customer and system requirements for mobile phone platforms and components, about 2 projects in parallel with 1000 - 2000 requirements each depending on project scope
- Participation in continuous improvement activities for requirements management and engineering
- Product Requirements Management
 - Overall responsibility for Requirements Repository and Documents
 - Gathering and elicitation of requirements/ needs from stakeholders
 - Requirements interface between the development team and internal and external customers/ stakeholders
 - Supports mapping of requirements to components
 - Monitors and tracks: quality of requirements and traceability
 - Drives requirement reviews
 - Requirements change handling/ participation in CCBs
 - Answers requests for information together with sales, marketing and technical experts
- Participation in continuous improvement activities
 - Alignment across platforms and customer projects in regular meetings
 - Provide customer requirements for reuse
 - Participate in continuous process and methodology improvement (TEC RE)
- Both internal and external interfaces operate on an international basis.
 - Internal: Business Line Marketing and System Engineering, Verification Management, Project and Program Management, Quality Management.
 - External: IFX customers and Network operators.

Requirements:

- Master in EE or equivalent
- 3 years + experience in relevant field
- Professional experience in System Engineering or related disciplines
- Good knowledge of IFX development processes with focus on System/ Product Definition is a plus
- Fluent in English
- Good expertise in Requirements Management

- Rational Requisite Pro
- MS Office (desirable including VBA)
- Adobe Framemaker (desirable)
- Social and communicative skills
- Self-organization

8. Logic Physical Synthesis Engineer Urgent!!!

Job Description:

- Interface with IC Design/Verification team (timing and power constraints definition)
- Writing, running, optimization of logic and physical synthesis scripts
- In-depth knowledge of STA. Ability to handle timing analysis for multiple modes and corners
- Physical design Floor planning, place & route, clock tree synthesis, routing cleanup
- Power IR & EM analysis
- Parasitic extraction/SPEF/SDF generation
- Prime Time/ICC STA correlation
- Formal Verification (Equivalence checking)
- Physical Verification (DRC, ERC, LVS, ANTENNA)
- Deep understanding of DSM effects (sub 90 nm experience preferred)

Requirements:

- Masters/Bachelor's Degree in Electrical/Electronics Engineering or in related field
- Tool skills:
 - Synopsys Design Compiler and Power Compiler
 - PERL, TCL languages
 - Prime Time and constraint creation/modification
 - IR analysis tool such as PrimeRail
 - Synopsys ICC experience preferred
 - Calibre and/or Assura
 - Formal Verification tool
 - Knowledge of VHDL or Verilog is a plus
 - RTL Hand-off checks (SpyGlass) and Design Doc. is necessary
- Ability to speak and write English is a must, CET 6
- Self-motivated team player and able to work with minimum supervision
- Minimum 2 years of physical design and timing closure experience
- Willingness to take overseas business trip

9. TD-LTE FW Development & Verification Engineer Urgent!!!

Job Description:

- Participate as a member of a challenging R&D team responsible for developing and maintaining complex Physical Layer Software of User Equipment to support TD-LTE & TD-SCDMA standard.
- Works include architecture design and detail implementation including test, release the fully functional solution on time and with very good quality.
- Works include analyzing, debugging complex scenarios in inter-operability tests & field tests, reproduce in low-level test and provide on time solution and with very good quality.

Requirements:

- Technical Background:
 - Deep understanding of TD-LTE & TD-SCDMA system, especially functionalities of physical layer
 - Long-term experienced SW Engineering with excellent C/C++ knowledge
- Soft skills:
 - Team work and Work independently
 - Able to work in a multi-national team
 - Problem solving and Fast learning
 - Good written and spoken English
 - Open to ask questions around