CORTINA SYSTEMS JOB OPPORTUNITIES

About Cortina Systems
Cortina Systems, Inc. is a leading provider of high-performance communications semiconductor solutions enabling next generation network connectivity and efficient bandwidth from the core network to the home network. Our broad product portfolio includes carrier-class semiconductor devices for next generation optical transport and passive optical network systems, as well as data center connectivity and digital home solutions.

Principal Member Technical Staff (Hardware Circuit Design)

Hardware Circuit Design Engineer position with strong emphasis in access networking and signal integrity knowledge. Thorough understanding of hardware design methodology, from product concept to design, layout, fab, assembly to test and debug. Will design test boards for Cortina semiconductor products and test chip performance at the system level.

Candidates will be proficiency in Orcad or DxDesigner, Allegro design tools. Proficient in simulation tools, Cadence, Hspice, sigrity, etc.

Proficient in the lab test equipment such as scopes, analyzers, data/signal generators, etc. to performing eye diagram measurements, jitter measurements, noise measurements, etc.

Required Qualifications:

BSEE in Electrical Engineering with minimum 8 years work experience in board level design.

Able to demonstrate knowledge in access, Ethernet, DDR2/3, Flash, VOIP, PON, Optical interfaces.

Understand Cadence, Hspice, PCBsi, or equivalent circuit simulation tools. Also, must be proficient in Orcad, DxDesigner and Allegro. Demonstrate proficiency with lab test equipment. Will be required to work to support overseas customers from time to time.

Preferred Qualifications:

Proficient in writing test scripts such as perl or verilog is a plus.

Principal Member Technical Staff (ASIC Design)

ASIC/SoC Design engineer responsible for concept-to-production design of +10mil gate high-speed networking devices incorporating EPON/GPON, Ethernet, and/or OTN standards.

Position and experience requirements:

- Work with Architect to analyze & comprehend design specifications, industry standards, customer requirements and applications to establish design and/or verification requirements and scope of work.
- Develop Micro-Architecture Specifications outlining design strategy, implementation and specifications
- Develop well structured, documented and synthesizable (Verilog) RTL code
- Provide input to verification plans outlining test strategy, environment, elements, test-cases and coverage goals to guarantee compliance to standards and functional requirements.

- Work with software team to validate the design on FPGA platform
- Work with verification engineers to debug RTL design code.
- Participate in design reviews of architecture, RTL, and verification environments/plans.
- Participate in back-end tasks such as static timing analysis, back-annotated gate level simulation.
- Participate in silicon bring-up.

Requirements:
Education / Experience Required for ASIC/SoC Verification Engineer:

- BSEE, Computer Science or Computer Engineering. MS (preferred).
- Minimum 8 years experience in state-of-the-art ASIC/SoC design and verification methodologies using Verilog and synthesis tools such as RTL compiler, also, formal verification tools and Tcl.
- Possess skills and aptitudes required to make and meet commitments; facilitate teamwork and communication with local and multi-site and/or multi-discipline development teams.

Principal Member Technical Staff (ASIC Verification)
In this position you will be responsible for the validation of access networking devices incorporating Ethernet, PON, L2/L3 Switch standards.
Responsibilities:

- Analyze & comprehend design specifications, industry standards, customer requirements and applications to establish verification requirements and scope of work.
- Develop verification plans outlining test strategy, environment, elements, test-cases and coverage goals to guarantee compliancy to standards and functional requirements.
- Architect, design, and implement (layered) self-checking environment using object-oriented strategies (with Vera) including behavioral functional models (BFM's), traffic generators and checkers to cover block and/or full chip verification.
- Develop test-cases using random, permutated and directed tests to assure standards compliancy, feature coverage and achieve functional & code coverage goals.
- Debug of RTL design code, environments, models, test-cases, scripts and tools.
- Script development (using Perl, shell scripting, C/C++) to control tools and post-process results and logs.
- Participate in design reviews of architecture, RTL, and verification environments/plans.
- Contribute to post-silicon validation including: strategy; test-case generation; test equipment identification and usage; device bring-up, test and debug.

Education Requirements:
BS degree in Electrical Engineering/Computer Engineering
MSEE/CE degree preferred
Minimum Experience Required:
8+ years experience in state-of-the-art ASIC/SoC design and verification methodologies using Verilog, Vera, System-Verilog, Specman and/or other equivalent object oriented programming languages. Must demonstrate track record in test plan development and test case implementation. Also demonstrate experience in verification model development using verilog/vera hardware language. Debug and bring-up the ASIC/FPGA in the lab.