

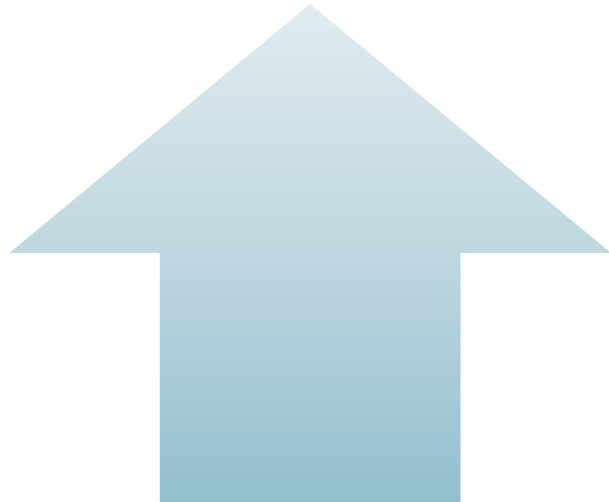
# Design Methodology Key to Semiconductor recovery and Economic Success

**Charlie Huang, Ph.D.**

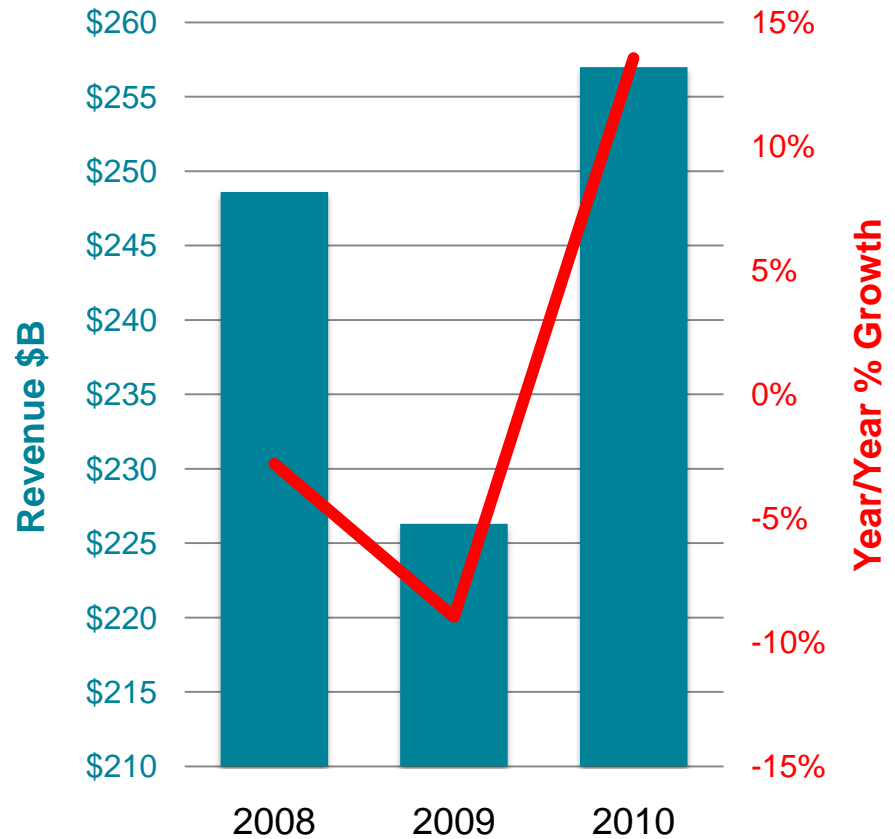
Senior Vice President and  
Chief Strategy Officer



# Semiconductor industry trend



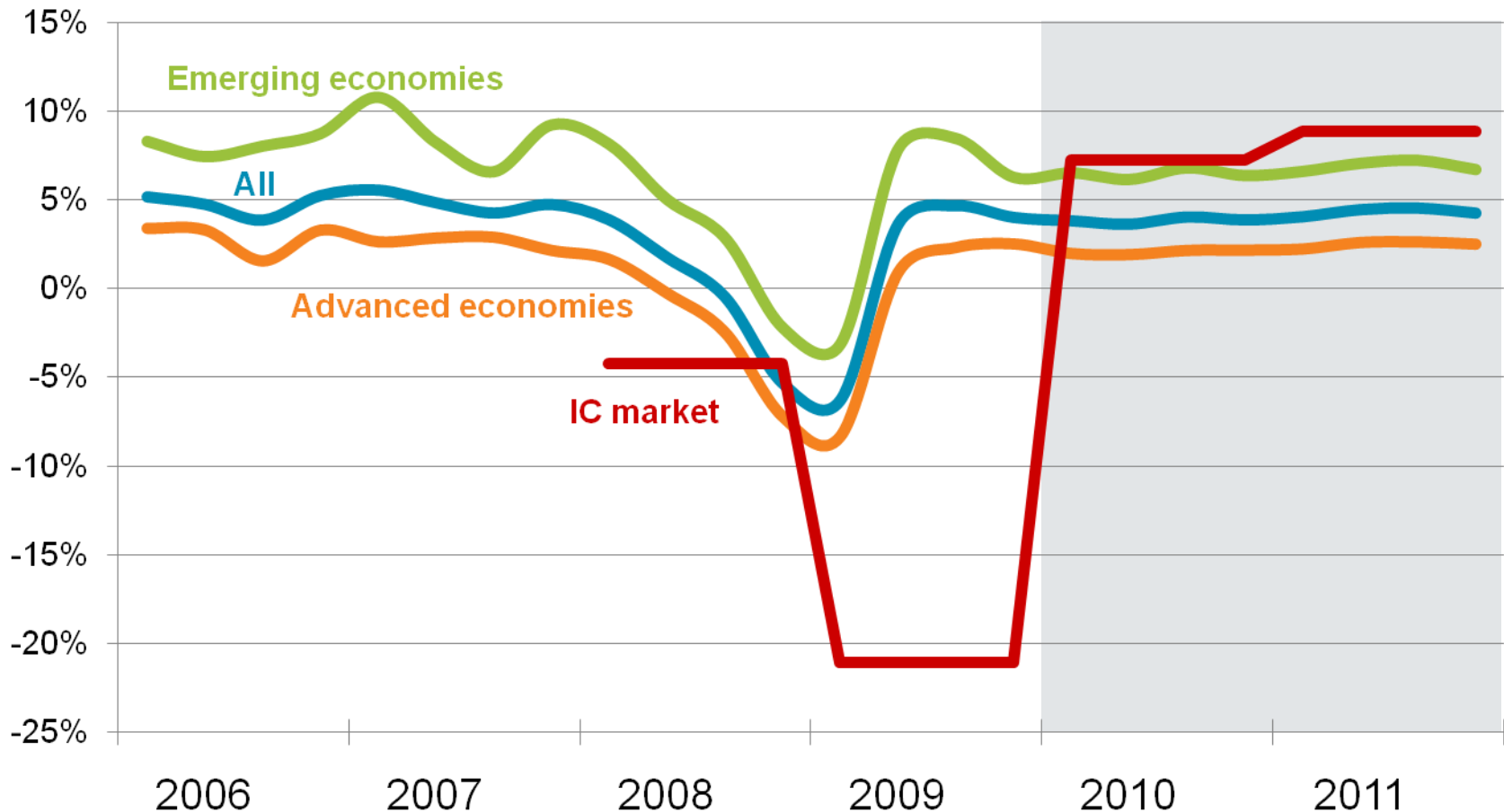
CELL PHONE  
AND COMPUTER  
UNIT SALES UP  
60% IN 2010  
(SIA)



Source: SIA and analyst forecasts

# IMF forecast for global recovery and WSTS forecast for semiconductor recovery

Percentage GDP growth, quarter-over-quarter, annualized



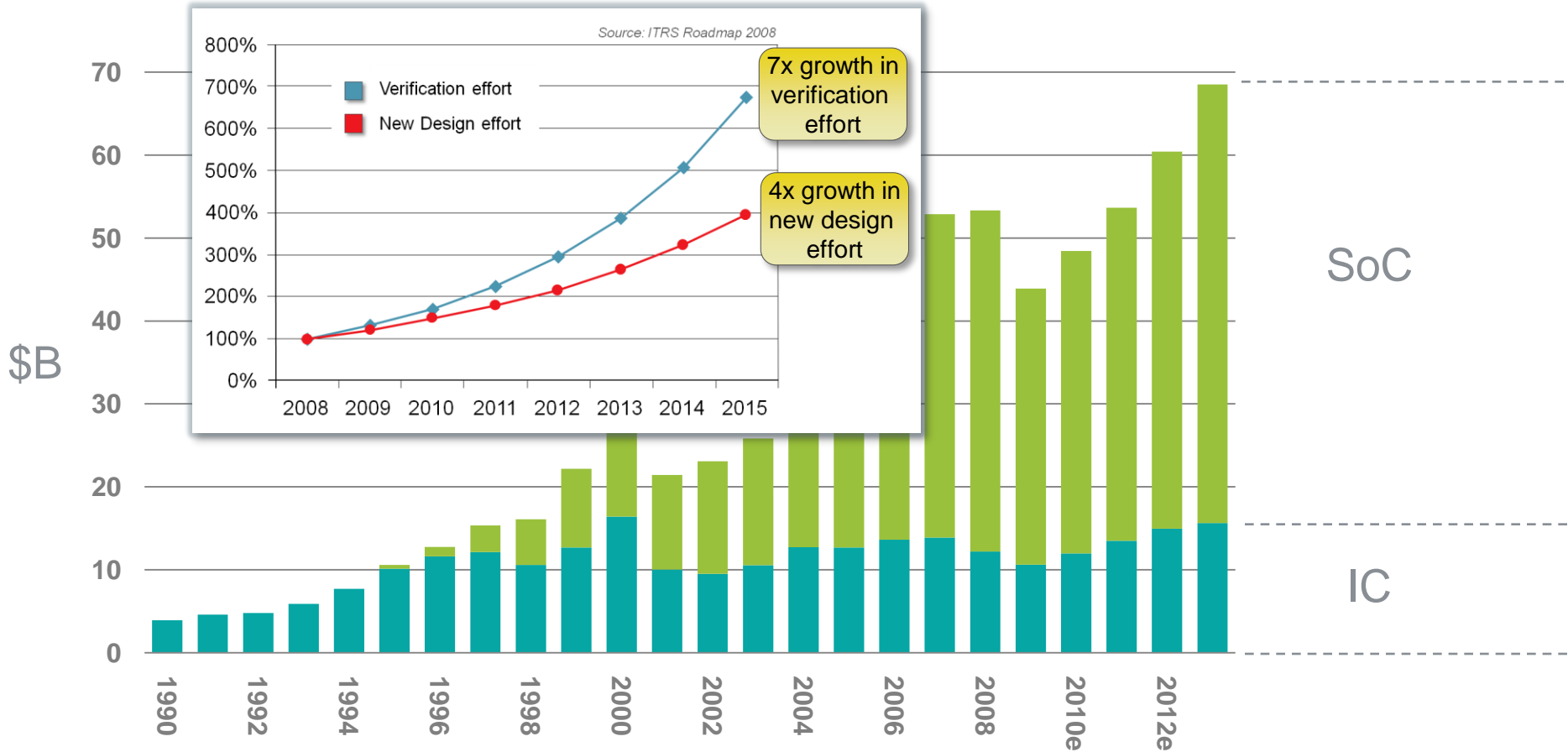
Source: WEO Update, January 2010

Source: WSTS Semiconductor Market Forecast, June 2009

# SoC drives semi industry revenue growth

Big design challenge –

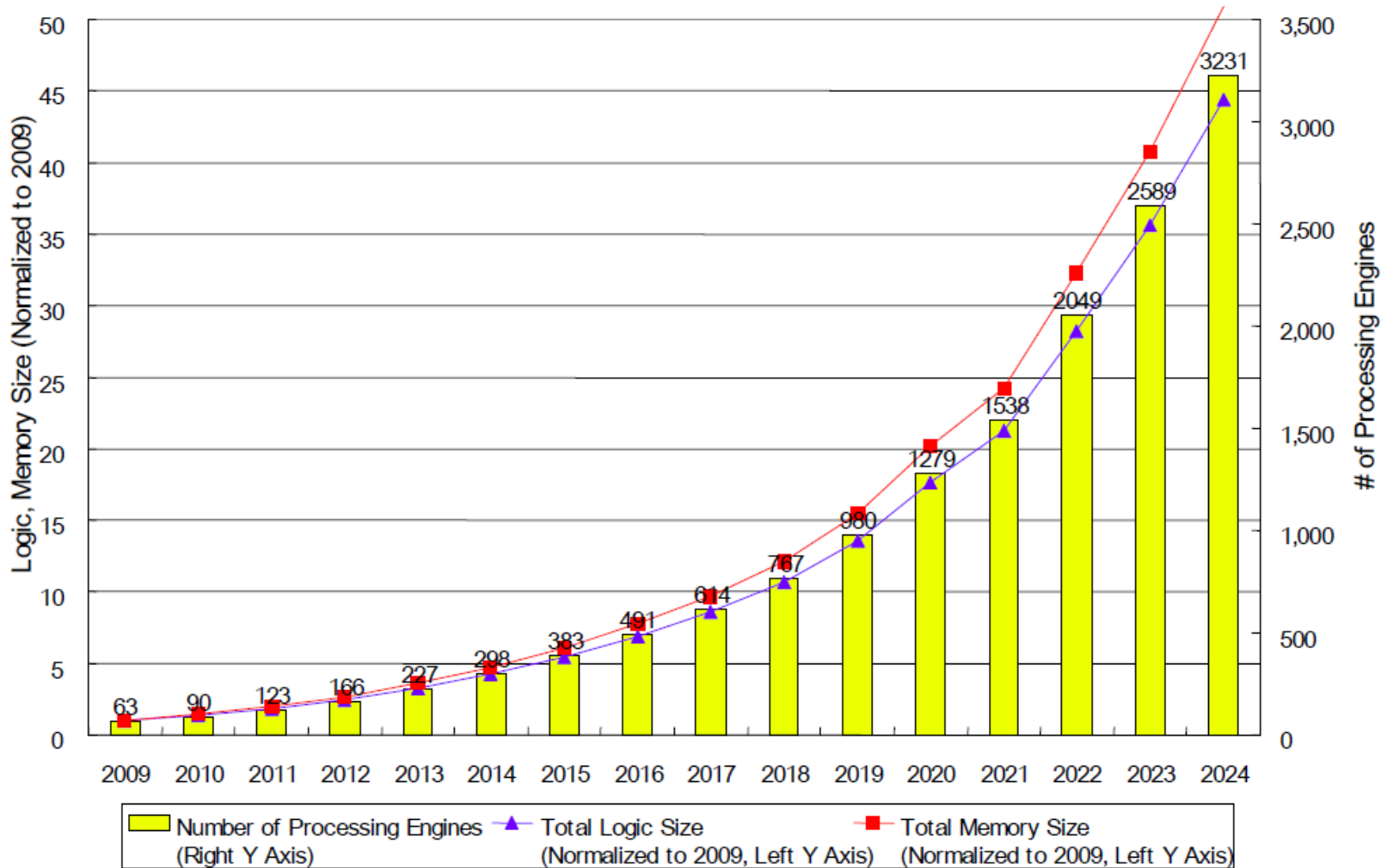
Bigger verification challenge



Source: Semico 2009

# SoC verification challenge grows

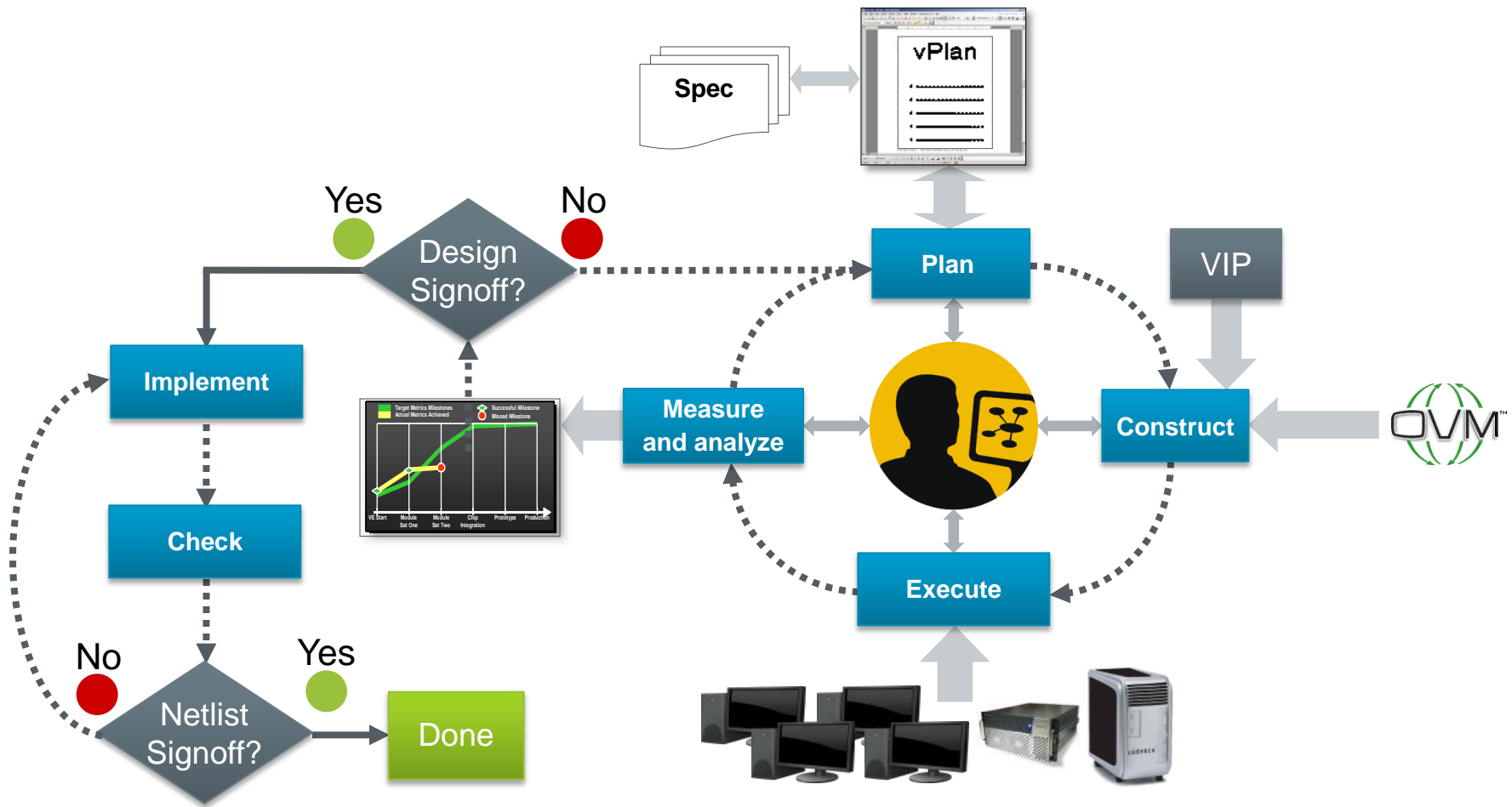
## Many cores, much more logic and memory



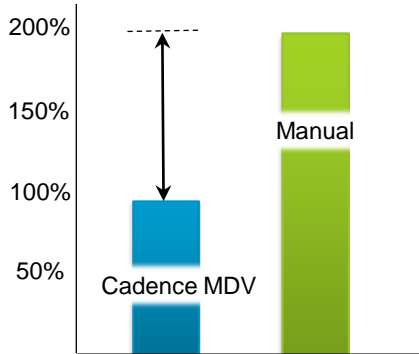
Source: ITRS 2009, System Drivers

# Metric-driven verification methodology

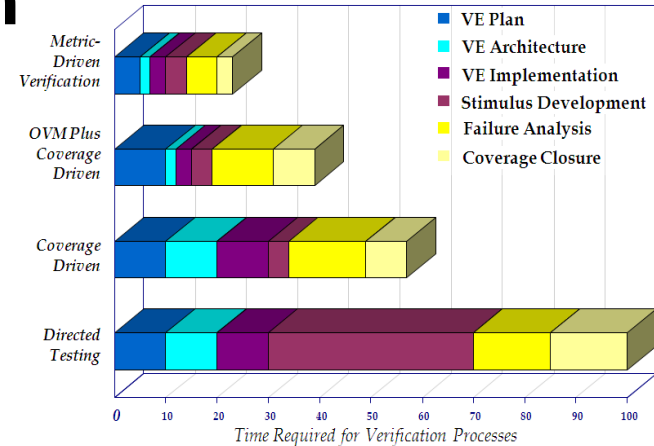
## Speeds design and reduces risk



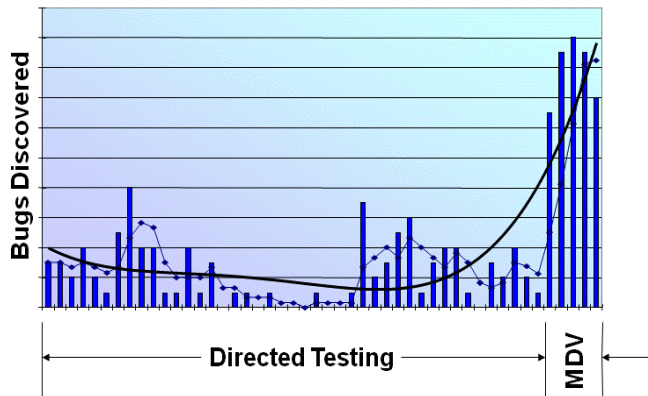
# Measurable advantages of metric-driven verification



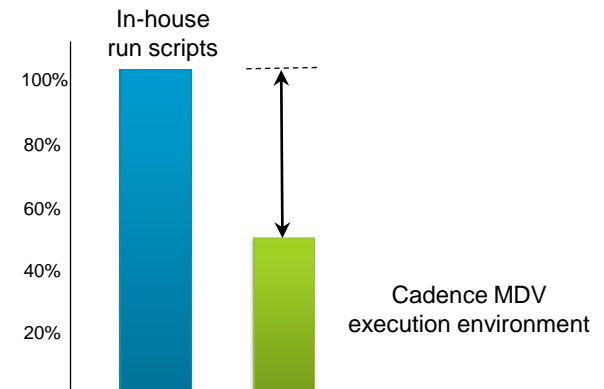
**Half the time of manual test planning and management**



**2x to 5x faster and more predictable verification closure**

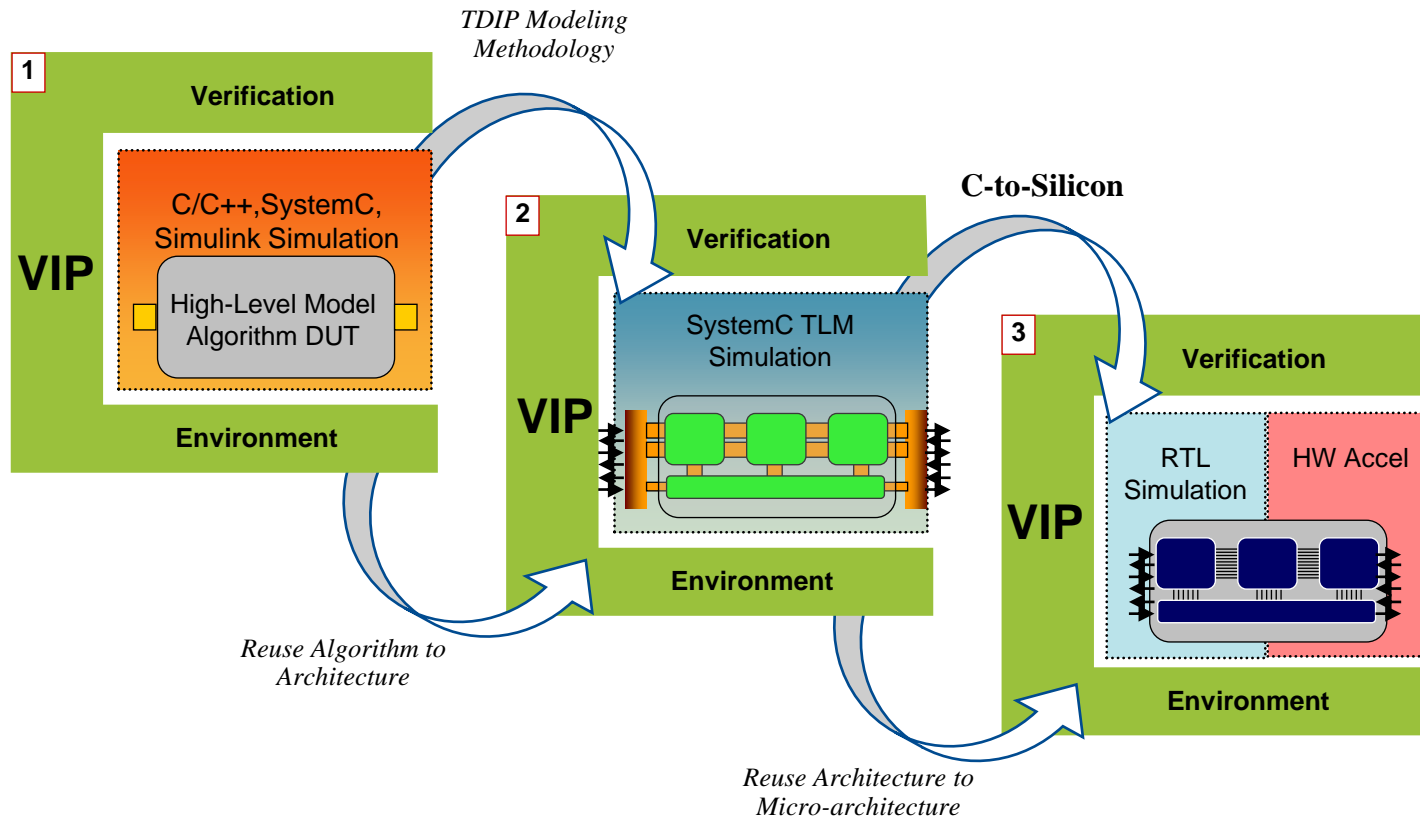


**Orders of magnitude more effective at finding bugs**



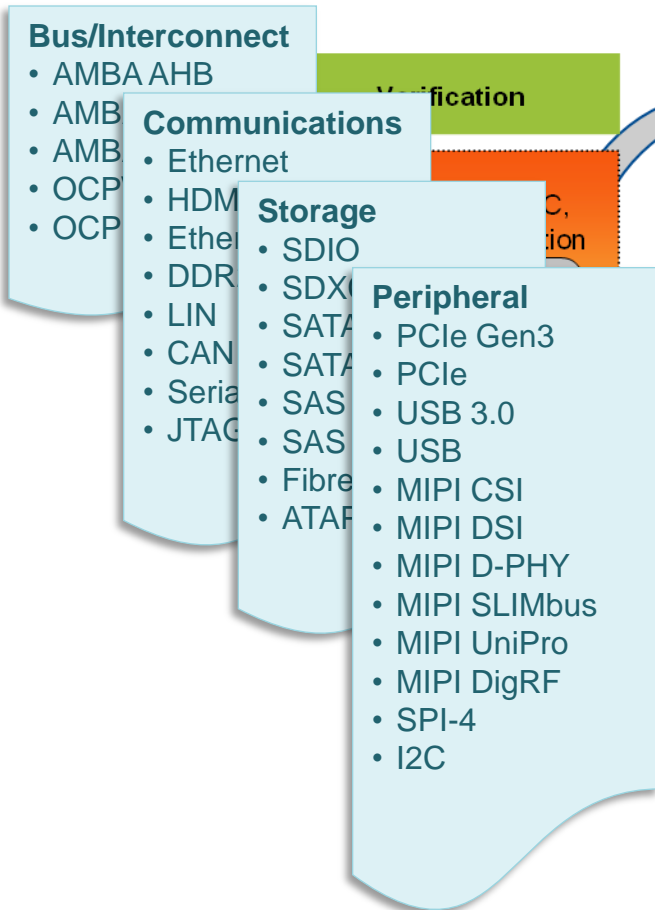
**50% lower regression maintenance over project duration**

# Utilize Verification IP (VIP) to speed design and reduce risk



# Utilize Verification IP (VIP) to speed design and reduce risk

## Broad Cadence portfolio



## Industry Standards



## Technical depth

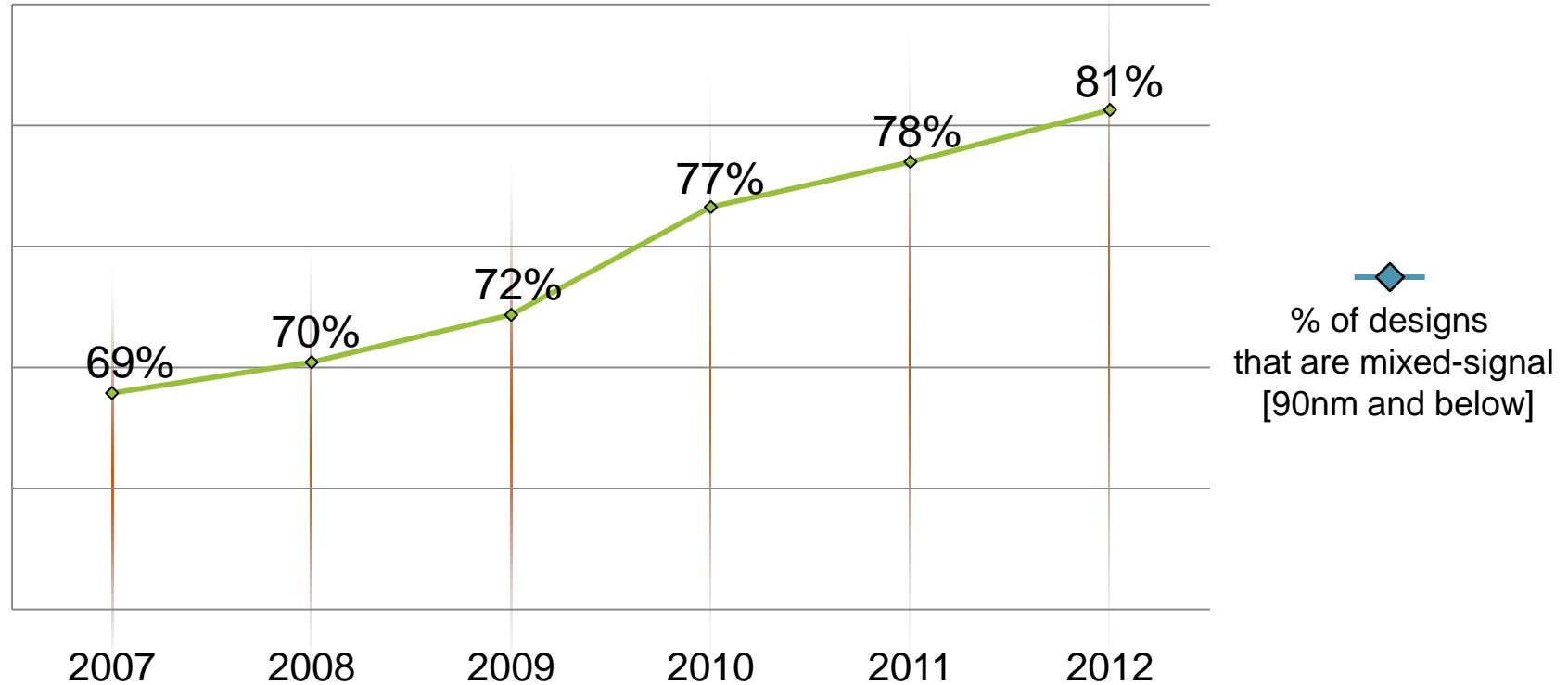
### Universal Verification Component (UVC)

- Verification depth
- Automated compliance management system (CMS)
  - OVM multi-language testbench interface
  - Complete protocol functional coverage
  - Constrained random test generation
  - Complete protocol checking
  - Bus functional model

### Integrated solution

- Built-in metric-driven verification**
- Delivers 2-10x greater productivity**

# Mixed-signal design is becoming more pervasive

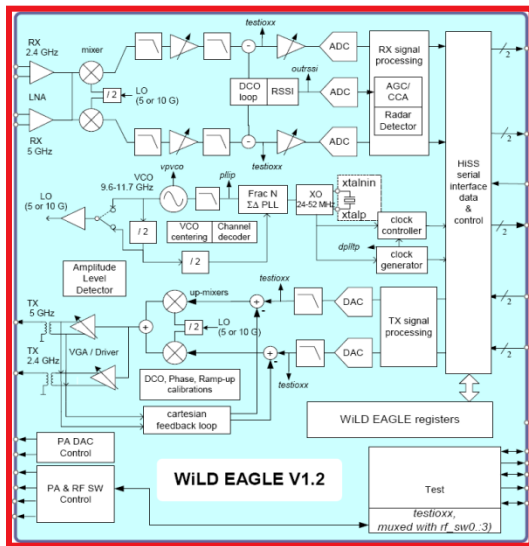


Source: IBS, June 2008

# Mixed-signal verification is complex

How do I verify the digital content in this SoC?

How do I verify the mixed-signal interconnects?

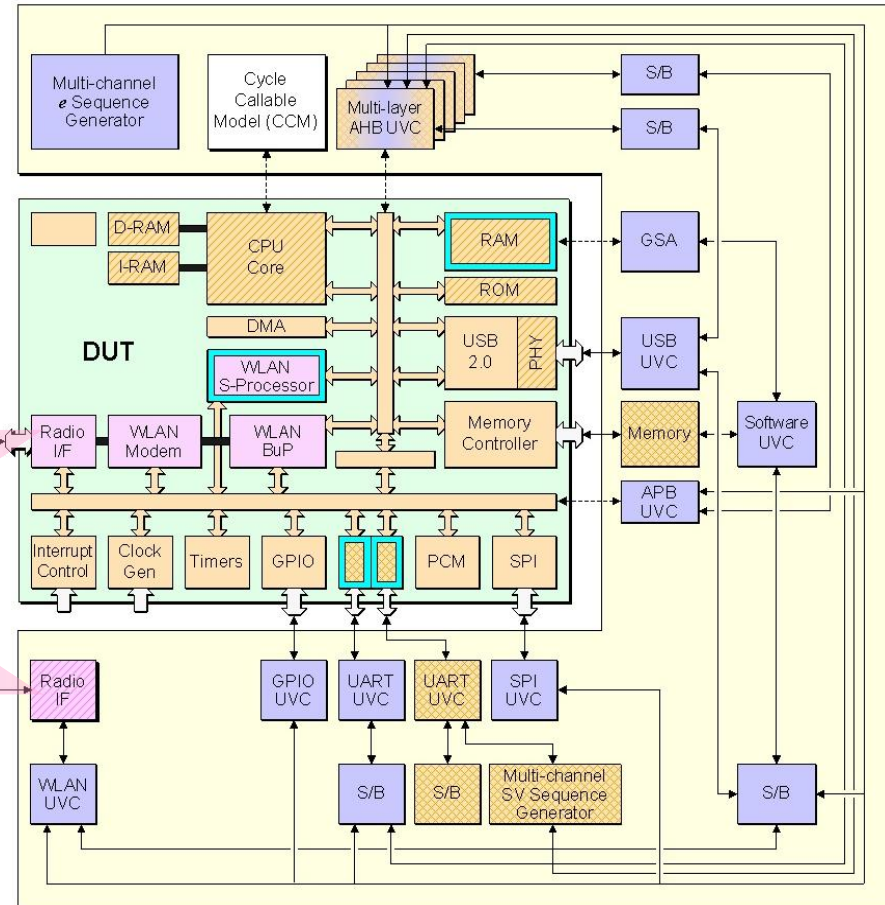


Design  
Analog Design  
Measure

How do I abstract analog behavior?

How do I verify the mixed-signal IP?

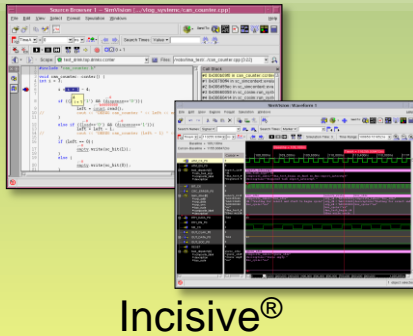
## Digital mixed-signal



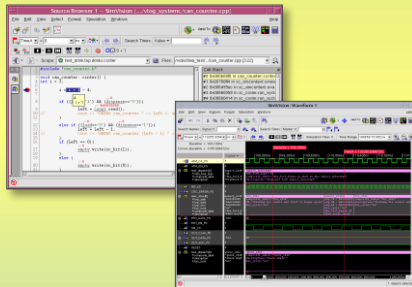
- Behavioral Verilog
- e
- TLM (SystemC)
- SystemVerilog
- Verilog RTL
- CCM (C)
- VHDL RTL
- S/B Score Board
- Behavioral VHDL

# Each domain has traditional approaches

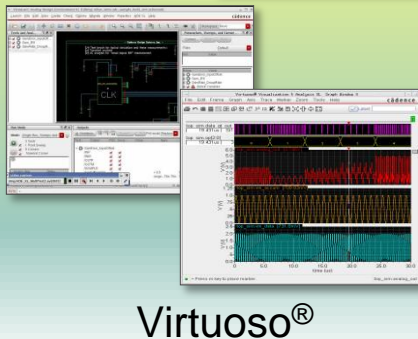
Digital



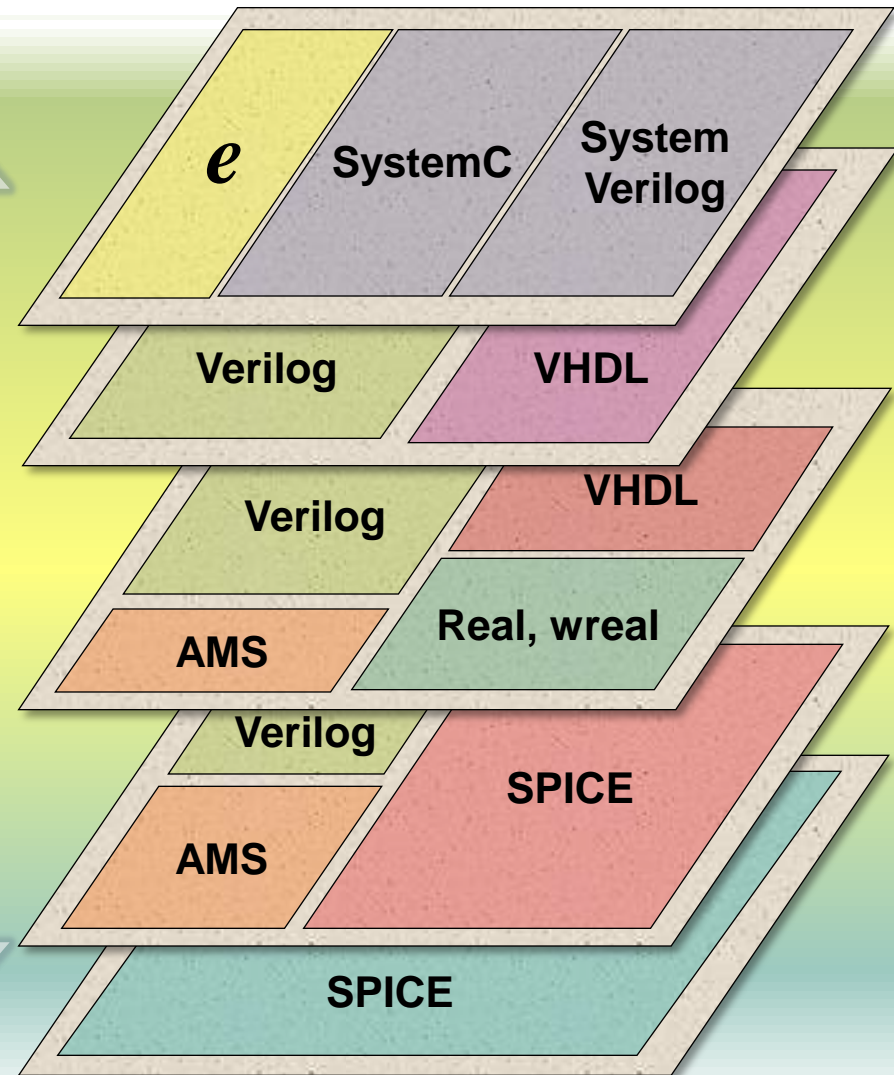
Mixed-signal



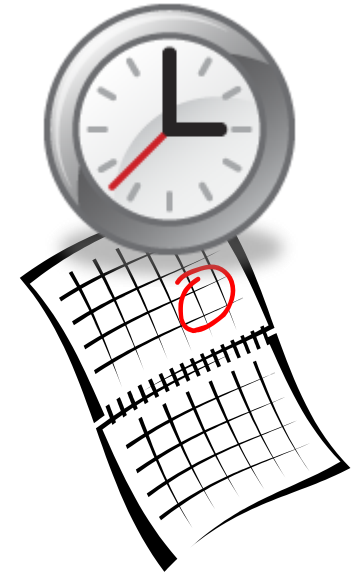
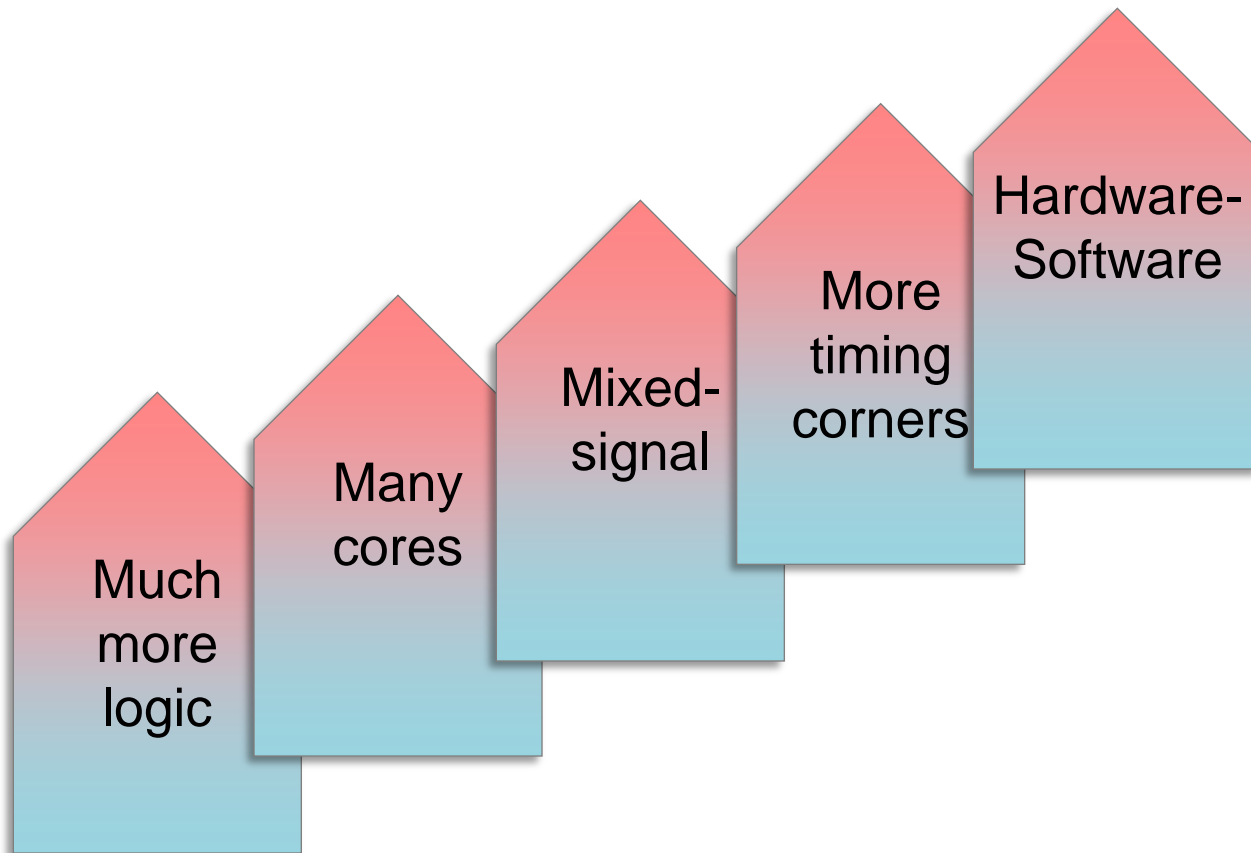
Analog



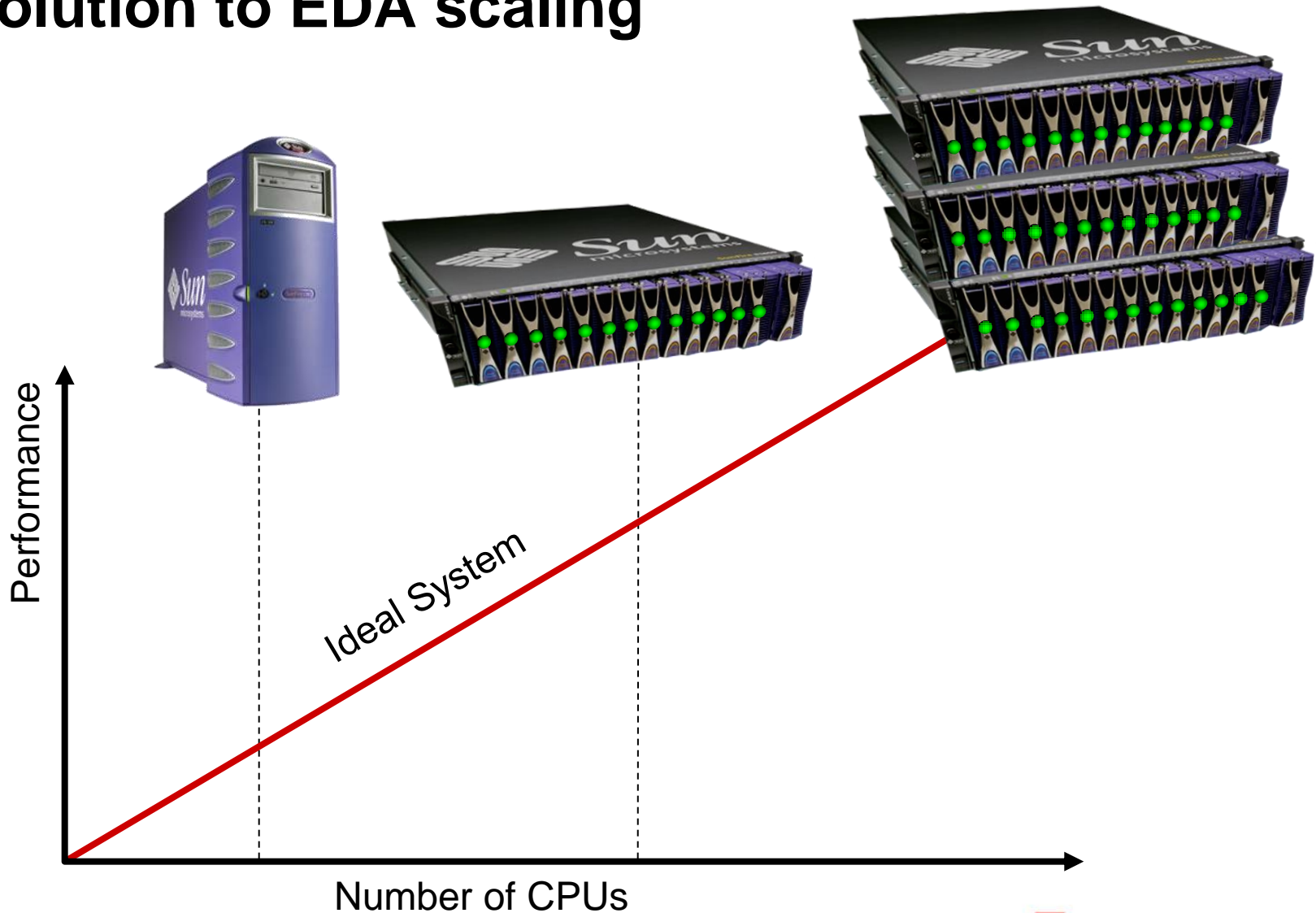
Mixed-signal verification



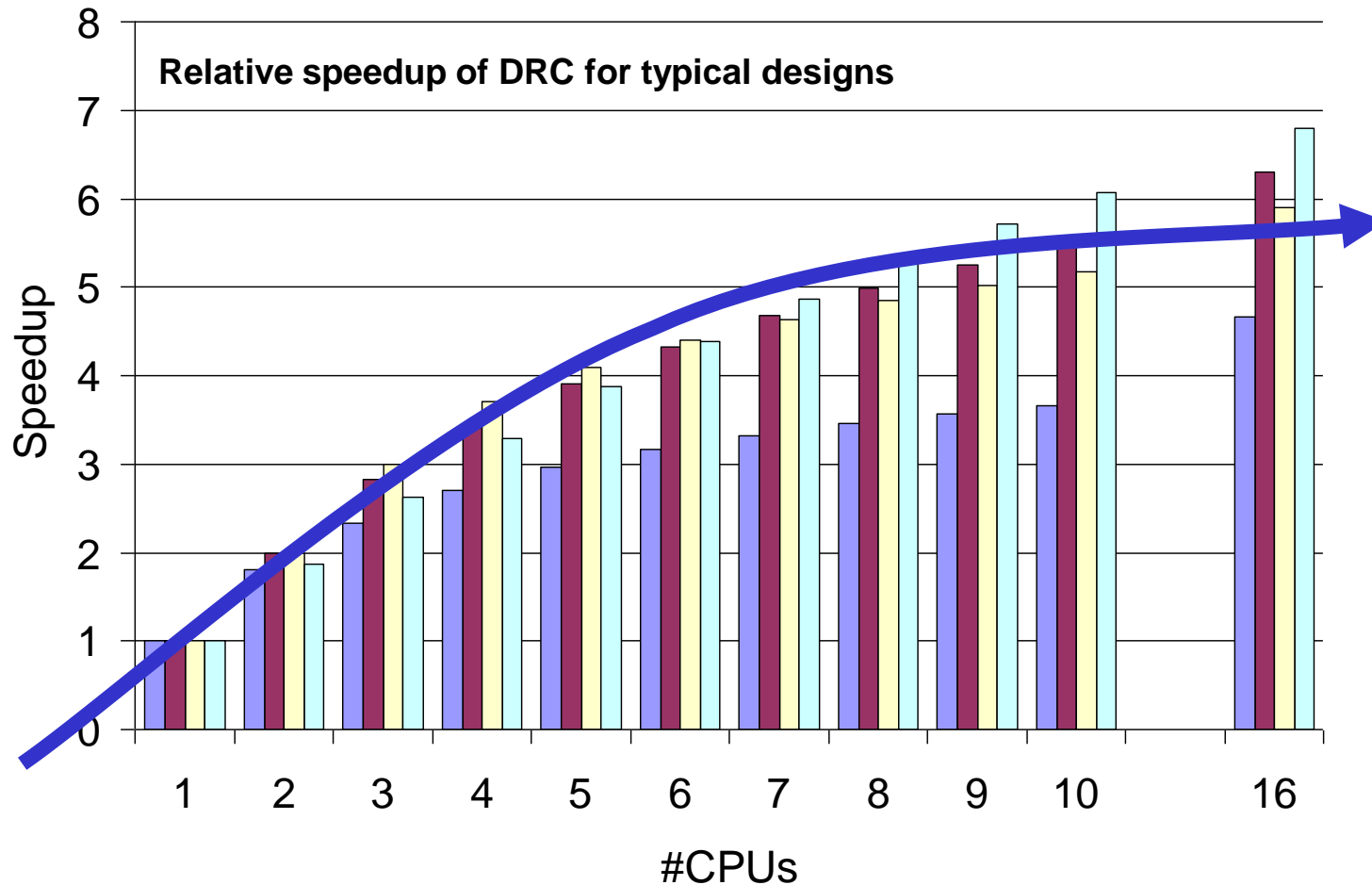
# Increased verification requirements mean increased compute loads – and increased delay



# Multi-core technology offers a solution to EDA scaling



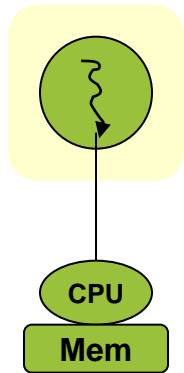
# But typical EDA tasks limit the scalability of multi-core approaches



# Success requires picking the right multi-core approach for each EDA task

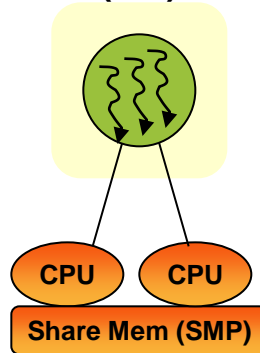
## Application Parallelization Models

Single threaded Application



Easy to develop and debug

Multithreaded Application (MT)



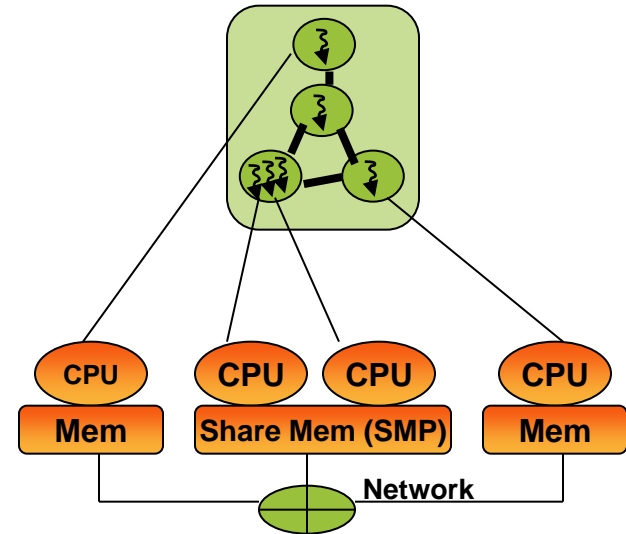
Shared Memory makes easy to thread/parallelize computations.

Thread synchronization needed

Scalability limited by hardware



Distributed Application (DP)



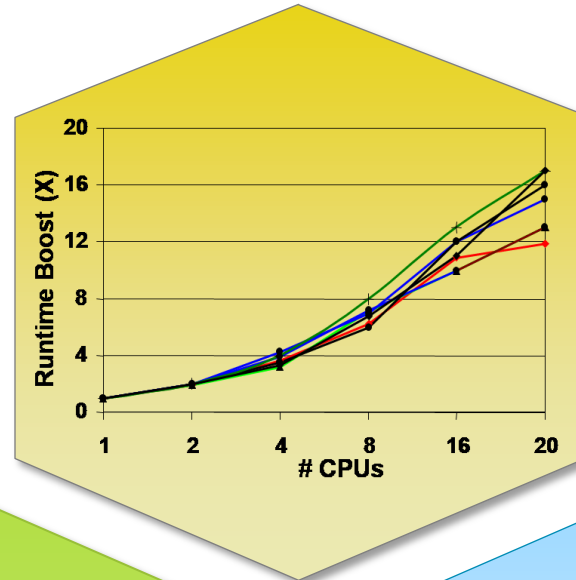
No shared memory. Connectivity by messages across network backplane

Requires application re-architecture work to synchronize computations due to lack of shared memory and crossing process boundary

Excellent scalability, performance, and design throughput

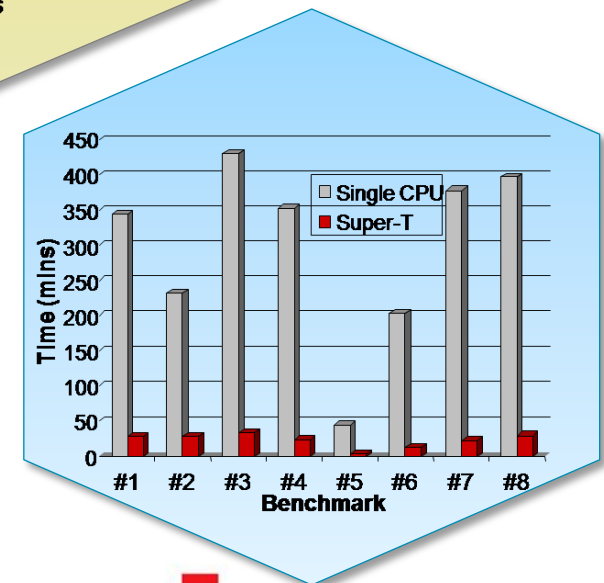
# Multi-core solution can approach linear scaling

## Example: NanoRoute SuperThreading

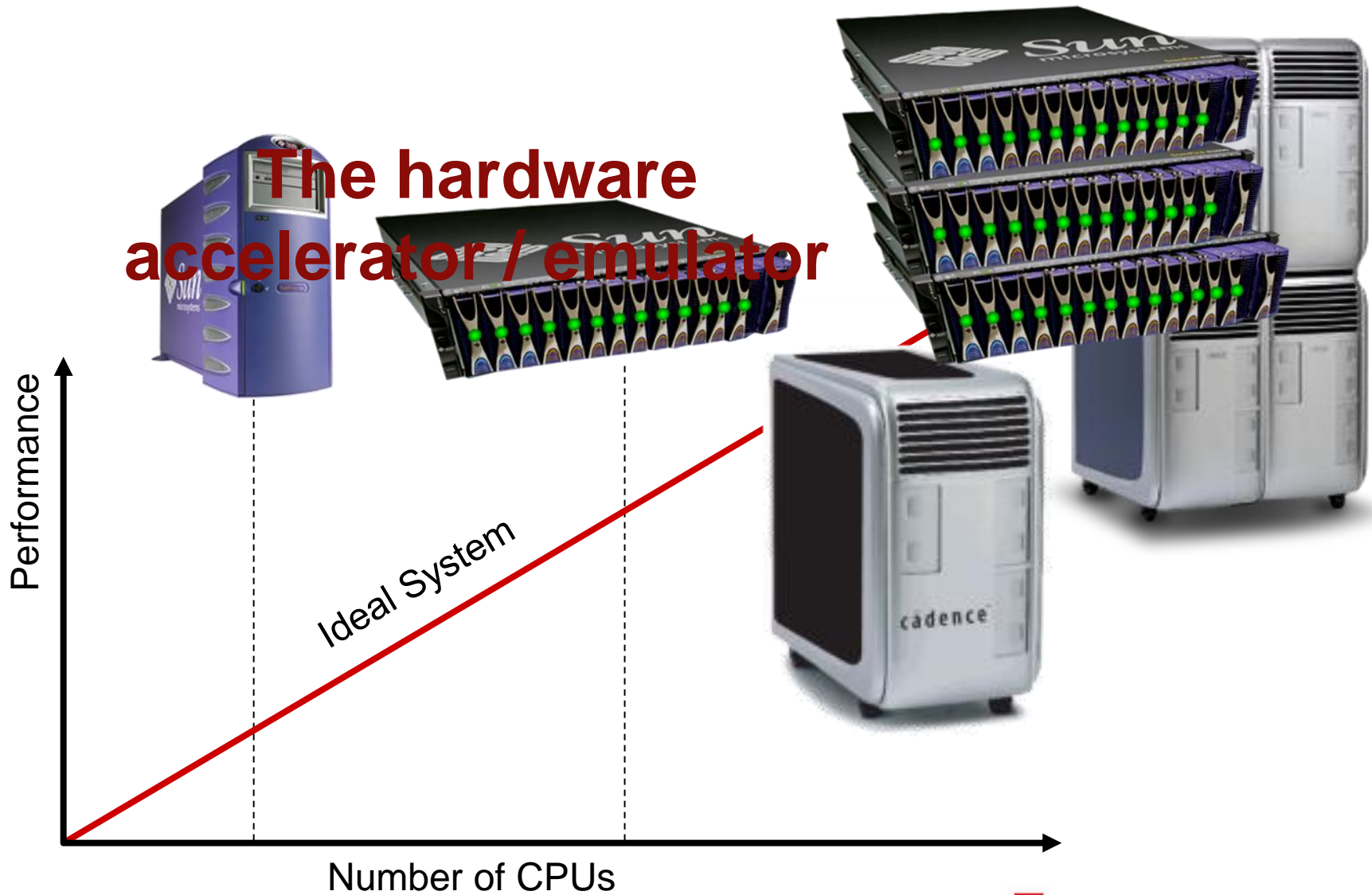


“We are seeing 10X runtime improvement on our designs without any special hardware.

Super threading takes NanoRoute performance to a whole new level and significantly reduces our design cycle without sacrificing quality.”



# The ultimate multi-core approach



# Summary

Process-node-driven design improvements are slowing,  
but design-methodology-driven design improvements  
are increasing

Different companies get radically different performance  
from the same processes

**For many companies, multicore technology  
and design methodology improvements have  
become more important than Moore's Law  
in meeting market requirements**



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