Chinese American Semiconductor Professional Association (CASPA)

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Silicon Valley
May 5, 2012 (Sat) 10:00 AM - 4:00 PM
Marriott Hotel, Santa Clara, CA
2700 Mission College Blvd, Santa Clara, CA 95054

Phoenix Arizona
May 7, 2012 (Mon) 4:30 PM - 9:00 PM
Fiesta Resort Conference Center
2100 South Priest Dr., Tempe, AZ 85282

We Share Vision and Values

Integrity Commitment Innovation Customer Partnership

About TSMC

Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC) is the world’s largest pure-play semiconductor foundry, and transformed the semiconductor industry with its pioneering business model of focusing solely on manufacturing customers’ semiconductor designs. Headquartered in Hsinchu, Taiwan, TSMC serves more than four hundred customers and manufactures over seven thousand products for them each year, almost 8 percent of global IC wafer shipments. In 2009, TSMC began pursuing further growth through new businesses, focusing on solar energy and LED lighting.

TSMC truly believes that talents are the cornerstone to reach ambitious goals in future, hence, has opened thousands of engineer/manager level vacancies to fresh graduate, experienced and overseas RDSS (研發替代役) in the fields of semiconductor technology R&D, IC design, manufacturing, IT, Finance, Accounting, Legal, etc.
Please note:

1. All the job openings are stationed in TSMC’s headquarters (Hsin-chu Science Park, Taiwan)

2. For pre-scheduled interview (if selected), please e-mail your resume to campus@tsmc.com, entitled “Degree_School_Major_Name_CASPA_available date of employment” and inform us the job fair you will be attending (Silicon Valley/Phoenix)

<table>
<thead>
<tr>
<th>Function</th>
<th>No.</th>
<th>Position</th>
<th>General Requirements</th>
</tr>
</thead>
</table>
| R&D              | R01 | 3DIC Process / Process Integration Engineer   | 1. Master or PhD in ECE, Physics, Chemical Engineering, Chemistry, Materials or related field.  
<p>|                  | R02 | Advanced Device Engineer / Manager            | 2. Work experience in related fields is a plus.                                         |
|                  | R03 | Advanced Module Engineer                     | 3. Willing to relocate to Hsinchu Science Park, Taiwan.                                 |
|                  | R04 | Novel Material (III-V) Module Engineer        |                                                                                      |
|                  | R05 | Advanced USJ Module Engineer                  |                                                                                      |
|                  | R06 | CIS (CMOS Image Sensor) Integration Engineer   |                                                                                      |
|                  | R07 | Embedded Memory Process Engineer              |                                                                                      |
|                  | R08 | HV Device Engineer                            |                                                                                      |
|                  | R09 | Lithography / Patterning Engineer             |                                                                                      |
|                  | R10 | OPC Engineer                                  |                                                                                      |
|                  | R11 | Packaging Manager                             |                                                                                      |
|                  | R12 | Power IC Engineer                             |                                                                                      |
|                  | R13 | SPICE Engineer                                |                                                                                      |
|                  | R14 | TCAD Engineer                                 |                                                                                      |
| IC Design        | D01 | 3DIC and Silicon Interposer Testing Methodology Design Engineer / Manager | 1. Master or PhD degree in EE, CS or related field.                                      |
|                  | D02 | ARM CPU SOC Design Manager                    | 2. Work experience in related fields is a plus.                                         |
|                  | D03 | Analog Circuit Design Engineer / Manager       | 3. Willing to relocate to Hsinchu Science Park, Taiwan.                                 |
|                  | D04 | Digital Circuit Design Engineer               |                                                                                      |
|                  | D05 | CAD Engineer                                  |                                                                                      |
|                  | D06 | Chip Implementation Engineer / Manager(APR)    |                                                                                      |
|                  | D07 | CIS (CMOS Image Sensor) Circuit Engineer       |                                                                                      |
|                  | D08 | DRC Engineer                                  |                                                                                      |
|                  | D09 | Physical Verification and RC Extraction Manager |                                                                                     |
|                  | D10 | Physical Implementation Engineer              |                                                                                      |
|                  | D11 | PHY(Physical Layer) Digital Design Technical Manager |                                                                                     |
| Manufacturing    | O01 | Advance Process Manager                       | 1. Master/PhD in EE, Physics, Chemistry, Materials or related field.                   |
|                  | O02 | Process Integration Manager                   | 2. Willing to relocate to Hsinchu Science Park, Taiwan.                                 |
|                  | O03 | Product Manager / Engineering                 |                                                                                      |
| IT               | I01 | IT Engineer                                   | 1. Master degree in IT.                                                                |
|                  |     |                                               | 2. Related work experience is preferred.                                              |
|                  |     |                                               | 3. Willing to relocate to Hsinchu Science Park, Taiwan.                                 |
| Finance/         | F01 | Finance Associate                             | 1. Master degree in Finance / Accounting / HR.                                          |
| Accounting       | F02 | Accounting Associate                          | 2. Related work experience is preferred.                                              |
| HR               | H01 | HR Specialist                                 | 3. Fluent in both English and Mandarin                                                |
|                  |     |                                               | 4. Willing to relocate to Hsinchu Science Park, Taiwan.                                 |
| TSMC Solid State Lighting | L01 | EpitaxyTechnical manager/Engineer             | 1. Master / PhD degree.                                                               |
|                  | L02 | Packaging / phosphor engineer                 | 2. Work experience in related industries is a plus.                                    |
|                  | L03 | Process/ Integration Engineer                 | 3. Willing to relocate to Hsinchu Science Park, Taiwan.                                 |
| TSMC Solar       | S01 | CIGS R&amp;D manager /Engineer                    | 1. Master /PhD degree.                                                               |
|                  | S02 | Equipment engineering manager                 | 2. Work experience in related industries is a plus.                                    |
|                  | S03 | Process Engineer                              | 3. Willing to relocate to Taichung Science Park, Taiwan.                                |
|                  | S04 | Product Development Manager                   |                                                                                      |
|                  | S05 | Product Engineer                              |                                                                                      |
|                  | S06 | Quality and Reliability Engineer              |                                                                                      |
|                  | S07 | Sales /marketing Engineer                     |                                                                                      |
|                  | S08 | Thinfilm Equipment Engineering Engineer        |                                                                                      |</p>
<table>
<thead>
<tr>
<th>Title</th>
<th>Responsibility</th>
<th>Requirement</th>
</tr>
</thead>
</table>
2. Define/refine advanced Logic technology offering.  
3. Guide customers for successful advanced Logic technology NTO and ramping.  
4. Roll out advanced Logic technology to regions | 1. Familiar with semiconductor process and device physics. Strong interest and good methodology to understand new product applications. Business related experience is a plus.  
2. Master or above preferred and specialized in semiconductor related field.  
3. Familiar with MS Word, Excel and PowerPoint and put data together in organized way.  
4. Fluent Mandarin and English.  
5. Team-oriented individual capable of working effectively with staff in sales, marketing, technology and operations;  
6. Excellent communication skills;  
7. Hands-on and an eye for detail;  
8. Ability to work and operate effectively in a very fast-paced environment; |
| Segment Marketing Manager | This position has responsibility to know one or multiple of MCU, Smartcard and mobile payment IC markets. Scope covers the related IC markets, vendors and eco-system, the IC function roadmaps and appropriate process technology mapping; to develop a total market wafer demand forecast; to know each customer’s position, the competitive market dynamics and IDM outsourcing trend/technology; and to develop and update demand forecast model. The job also needs to provide segment and customer strategies. | 1. BS/MS major in EE or CS  
2. Over 10 years of working experience in product manager or marketing role in MCU, Smartcard or embedded-Flash related markets in IC or system companies  
3. With domain knowledge in technology and/or market research.  
4. Strong modelling capability  
5. MBA and has been working in IDMs is a plus |
| CIS System/Module Integration Manager | 1. Establish and maintain Image Module Technology roadmaps;  
2. Establish fully integrated image system & enable imager performance confirmation extended from Silicon level to the Camera Module level;  
3. Drive team for camera module quality evaluation, develop & establish module Device Verification Test (DVT) solutions;  
4. Work with lens vendors to develop lenses for imager test chip demonstration, and develop advanced lens technology for special optical applications;  
5. Work with both internal & external package expert groups to develop lenses for imager test chip demonstration, and develop advanced lens technology for special optical application. | 1. BSEE or MSEE or related fields is highly required;  
2. Strong image sensor and camera module knowledge base;  
3. Minimum 10+ years design and production experience for the camera module for Mobile Phone, PC/Web Cam, or DSC applications;  
4. Minimum 5 years management experience;  
5. Direct package assembly manufacturing experience preferred.  
6. Ability to manage priorities and be flexible;  
7. Solid knowledge base & good experience on camera module bonding, assembly and optical performance;  
8. Proven leadership skills and ability to motivate others.  
9. Need to work at Taiwan |
| III-V Epi Technical Manager | 1. Development of epitaxial III-V compound semiconductor growth by means of MOCVD  
2. Responsible for the maintenance and further enhancement of the epi processes & equipments  
3. Work in close collaboration with Integration to optimize the device performance, reliability, and yield.  
(Reporting to Senior Technical Manager of Specialty Module Division) | 1. PhD in Physics, Materials Science, Chemical, and Electrical Engineering with strong scientific skills.  
2. At least 7+ years of industrial experience in working with Si epitaxy, III/V or III-nitride MOCVD or Molecular Beam Epitaxy is required.  
3. An ambitious and motivated team player with good communication and reporting skills. |
<table>
<thead>
<tr>
<th>Role</th>
<th>Responsibility</th>
<th>Requirement</th>
</tr>
</thead>
</table>
| **Device Technical Manager**              | 1. Responsible for projects of advanced device technology development, device target setting, scheme definition, simulation, and characterization.  
2. Coordination among Device, Integration, and Module in R&D.  
3. Planning and setting priority for execution on customer request and delivery schedule.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 1. At least 5 years experience in process integration or device development.  
2. PhD or MST degree in Electronics Engineering or Physics field  
3. Minimum 5 years of experiences in device technology development  
4. Fluent in English (fluent in Mandarin is a plus)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| **Physical Implementation for RTL-GDS design, Technical Manager** | 1. Lead physical implementation and performance innovation tasks  
2. Define and provide solution for Ghz design flow including high speed clock tree synthesis, SBOCV optimization and sign-off methodology  
3. Define and provide solution for low power design flow including circuit innovation, DVFS implementation and sign-off methodology                                                                                                                                                                                                                                                                                                                                                              | 1. Mater in EE/CS related field, at least 10+ years of industrial experience  
2. Familiar with EDA Auto P&R skill  
3. Familiar with RTL-GDS design flow with real project experience  
4. Expert of design solution for high speed or low power design  
5. Accountability and willing to take challenging tasks  
6. Experience on Physical implementation, timing closure, DRC/LVS check, high speed and low power design flow                                                                                                                                                                                                                                                                                                                                                                                  |
| **CPU Front end technical Manager**       | 1. CPU core front end design flow including RTL synthesis, DFT/MBIST implementation and SoC/Test chip integration and verification  
2. Test chip silicon measurement including ATPG/functional pattern generation, debugging and measurement data analysis                                                                                                                                                                                                                                                                                                                                                                                              | 1. Master degree in EE/CS related field, at least 7+ years of industrial experience  
2. Familiar with chip implementation design flow  
3. Familiar with chip silicon measurement  
4. Familiar with low power/high speed RTL coding and synthesis skill is plus  
5. Key experience on Low power/high performance RTL code analysis, MBIST/DFT implementation, High speed RTL synthesis, SoC/test chip verification, Chip debugging and measurement                                                                                                                                                                                                                                                                                                                                                   |
| **Design Application & support Manager**  | 1. Act as DTP contact window to be responsible for the following design support of TSMC key customer and worldwide FTS/FAE  
   a. Lib/IP Support  
   b. EDA tools and design flow support  
   c. RTL or Netlist to GDS design backend support  
   d. DFM support  
2. One team Program Manager to coordinate RD, PE and DTP to provide regular support and complete solution to strategic accounts.                                                                                                                                                                                                                                                                                                                                                          | 1. M.S. degree or above in EE with a minimum of ten years of working experience in IC or design related field.  
2. Minimum 5 years of experience in IC design companies, either in design or FAE roles. Those with solid knowledge of the IC industry technical service or IC design would be advantageous.  
3. Proven capabilities in strategic customers service skills, cross culture negotiation, excellent presentation skills and leading service team would be preferred.  
4. Familiar with IC design, methodology, library/IP, EDA industries and tools.                                                                                                                                                                                                                                                                                                                                                                               |
| **DFT and diagnosis for advanced process technology & 3D IC** | Role: Project leader  
1. Define DFT and diagnosis structure for advanced process technology & 3D IC  
2. Implement defined structure for TSMC 2D/3D test vehicles for yield learning  
3. Provide solution for 3D IC testing flow including KGD, KGS solution of bottom die, stacked die, WideIO DRAM, HMC(hybrid memory cube), HBM(high bandwidth memory), and silicon interposer  
4. Innovate solution of DRAM MBIST/repair, diagnosis and PFA for advanced & new process technology  
| 1. Ph.D in EE related field  
3. 3D IC Design for Test solution such as IEEE P1838, P1500  
4. Reviewer in the DFT conference committees and lead in DFT solution provider  
5. Expert in DRAM MBIST/repair, diagnosis, PFA and yield learning  
6. Rich in paper, patent publication and submission (First author preference)  
7. Key experience in 3D IC, DFT (design for test), DRAM MBIST/repair, Diagnosis, yield learning  
8. Creative and willing to take challenging tasks                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| **EDA Marketing Manager**                 | Role: EDA Eco-system Partner Management Responsibility:  
1. Engaging EDA eco-system partners  
2. Product marketing of TSMC Open Innovation Platform  
3. Collaborating with EDA eco-system partners to support common customers  
| Requirement:  
1. Deep understanding of EDA industry in terms of business and technology  
2. Strength in initiating, organizing and driving cross department collaboration  
3. Superior technical strength in EDA and IC Design  
4. Superior interpersonal skill  
5. Over 8 years of industry experiences in the field of IC design and EDA  
6. Master Degree in EE  
| Language:  
Superior command in English for extensive daily communication with English-speaking only EDA partners  
<p>|</p>
<table>
<thead>
<tr>
<th>Role</th>
<th>Responsibility</th>
<th>Requirement</th>
</tr>
</thead>
</table>
| Efuse Technical Manager                   | 1. Efuse circuit design  
2. Custom efuse macro design                                                                                                                   | 1. MST EE and above  
2. 8–10 years working experience  
3. Familiar with customized circuit design flow  
4. Good English communication skill  
5. Personal Attributes: Innovation, Self-motivated, Problem solving oriented, Team work oriented |
| Speciality Technical Manager (CIS, Power IC) | 1. Leading the team for the process integration and new product development and ramp up  
2. New technology or customized technology transfer, installation, qualification, volume production ramping and sustaining smooth production  
3. Device uniformity and yield improvement/enhancement  
4. XFab device matching.                                                                 | 1. MS degree or above in Electric Engineering, Material Science, Physics. Etc. Concentration in Device related field is plus  
2. Needs domain knowledge of electronic and semiconductor industry in CIS or Power IC  
3. Specialist who owns strong problem solving experience and keen on solving outstanding issues is welcomed  
4. Fluent English or Mandarin speaking, good listening and writing for effective internal communication among PE, R&D  
5. 10+ years in semiconductor field and most preferably have at least 5 years device experiences. |
| Packaging Technical Manager               | 1. Be a leader in supporting the transfer of advanced package interconnects technology from RD into Operations, their qualification, and mass production bring-up at in-house facilities  
2. Lead and manage in-house package engineering development activities to support Si interposer, flip chip, 3DIC and related customer products and internal programs. | 1. At least a Master degree in Engineering field. Materials science or engineering, mechanical engineering, and related disciplines are preferred  
2. >10 years experience in advanced IC package engineering and high volume IC package operations management  
3. Strong knowledge in the area of wafer level packaging, flip chip, substrate, their materials, and integration is essential. Experience in 3DIC packaging and process technology is a plus  
4. Good English skills (verbal and writing) is critical. |