

2011 CASPA / Critical Talent

MediaTek Inc. is a leading fabless semiconductor company for wireless communications and digital multimedia solutions. The company is a market leader and pioneer in cutting-edge SOC system solutions for wireless communications, high-definition TV, optical storage, DVD and Blu-ray products. Founded in 1997 and listed on Taiwan Stock Exchange under the code "2454", MediaTek is headquartered in Taiwan and has sales and research subsidiaries in Mainland China, Singapore, India, U.S., Japan, Korea, Denmark and England. For more information, please visit MediaTek's website at www.mediatek.com

To Apply

Please send your resume to recr@mediatek.com and state the position/work location that you would like to apply in the subject. Thank you.

Job Position

Power Management System SW Architect

Job Location

San Jose

Job Description

The Senior Power Management Architect, as a member of the System Performance & Architecture Team of Mediatek, Inc., is responsible for generating the highest level of right software architecture for power and thermal management covering both software and hardware aspects to support MediaTek mobile product developments. Specific responsibilities may include the following:

1. Collaborate with product marketing and cross-functional teams to define performance, power and thermal requirements and guide the development of advanced low power technology to deliver long battery life solution for mobile products
2. System power analysis and control architecture analysis of mobile SOC
3. Promote performance, power and thermal development (both HW & SW) from design to implementation with a goal to improve the robustness of system controls
4. Make recommendations on system power architecture in relation to hardware and software structures
5. Drive the HW/SW low power roadmaps & strategies for mobile products

Job Requirements

1. More than 10 years direct experience with a proven track record within mobile phone industry
2. Possesses master above degree
3. Sensitive insight on novel low power and thermal technique and development trend
4. Experienced in power distribution units and power managements in mobile devices
5. Experienced in power and thermal modeling and analysis for mobile devices
6. Strong background in SW and HW system architectures with design experience at the SOC/chipset level is a plus
7. Excellent programming skills in C and C++ with experiences in embedded systems design & development desired
8. Experience in task and priority management across various engineering functions and cross-functional teams
9. Familiarity and experience with Linux and/or Android operating systems
10. Computer architecture domain general knowledge and background in digital and IC design
11. Excellent verbal and written communication skills and the ability to take initiative with sophisticated assignments
12. Working in Taiwan is preferred

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Job Position

System Power Platform Architect

Job Location

San Jose

Job Description

The System Power Architect, as a member of the System Performance & Architecture Team of Mediatek, Inc., is responsible for generating the highest level of right platform architecture for system power and thermal management including SOC and surrounding system to support MediaTek mobile product developments.

Specific responsibilities may include the following:

1. Make recommendations on performance, power and thermal development (both HW & SW) from design to implementation with a goal to improve the robustness of system controls
2. Collaborate with product marketing and cross-functional teams to define power requirements and guide the development of power management.
3. System power analysis and control architecture analysis of mobile SOC
4. Drive the HW/SW low power roadmaps & strategies for mobile products

Job Requirements

1. More than 10 years direct experience with a proven track record within mobile phone industry
2. Master above degree in EE
3. Strong background in PMIC development is required.
4. Sensitive insight on novel low power and thermal technique and development trend
5. Experienced in power distribution units and power managements in mobile devices
6. Experienced in power and thermal modeling and analysis for mobile devices
7. Strong background in SW and HW system architectures
8. With design experience at the SOC/chipset level is a plus
9. Experience in task and priority management across various engineering functions and cross-functional teams
10. Computer architecture domain general knowledge and background in Analog IC design
11. Excellent verbal and written communication skills and the ability to take initiative with sophisticated assignments
12. Working in Taiwan is preferred

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Job Position

Low power Hardware Architect (Covering PMIC bottom up requirement)

Job Location

Austin

Job Description

1. Collaborate with internal cross-functional teams to define and architect SoC low power technologies for best-in-class SoC power reduction and performance boost solutions for 28nm and 20nm technology nodes and beyond.
2. Drive the circuit, IP, and SoC design, development and deployment of the low power technologies for a scalable solutions between power and performance.
3. Provide analysis, recommendation and development of the autonomous low power technology solutions
4. Define power and MHz entitlement direction, execution and achieve next-generation low-power innovations' benefits for Ultra-Low-Voltage (ULV) scaling for voltage-frequency-power entitlement.

Job Requirements

1. Ph.D. EE or equivalent with 15+ years of SoC design experience
2. 7+ years of low-power & high-performance technology innovations, SoC design, development, and production experience required.
3. Production experience with leakage reduction, AVS, DVFS technologies is required.
4. Hands-on low-power SoC, from architecture, spec, design, to production experience required.
5. Advanced next-generation low-power architecture and development experience is preferred.
6. Strong communication skills is a plus.

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Job Position

Sr. Designer for SoC integration
(Speed Binning)

Job Location

Hsin Chu, Taiwan

Job Description

1. Mobile SOC integration, design for speed binning
2. low power design, DVFS, AVS, ABB, multi-Vt, MTCMOS
3. On-chip critical path emulator and Thermal meter

Job Requirements

5+year hand-on working experience on the speed binning chip and system testing design

Nice to have:

1. Experienced in CPU chip and system level testing speed binning
5. Experienced in CPU Speed gap debugging

Already hands-on speed binning design on chip is a big plus

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Job Position

Design Manager for Task Force Lead (Speed Binning)

Job Location

Hsin Chu, Taiwan

Job Description

1. SOC speed binning and debugging
2. Correlating and trouble-shooting design MHz/power target vs. silicon
3. Low level circuit knowledge, such as process variation, cell library, SRAM, PI/SI, static & dynamic IR-Drop
4. low power design, DVFS, AVS, ABB, multi-Vt, MTCMOS, etc
5. Thermal and low power meter design and debugging
6. Already hand on the low power and thermal design is a big plus to this job opening

Job Requirements

1. MSEE or equivalent plus 10+ years industry experience required
2. Strong communication skills preferred.
3. Managing experience is a plus

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Job Position

Sr. Designer for CPU PD/CPU critical path Opt (Speed Binning)

Job Location

Hsin Chu, Taiwan

Job Description

1. SOC speed binning and debugging
2. Correlating and trouble-shooting design MHz/power target vs. silicon
3. Low level circuit knowledge, such as process variation, cell library, SRAM, PI/SI, static & dynamic IR-Drop
4. low power design, DVFS, AVS, ABB, multi-Vt, MTCMOS, etc
5. Thermal and low power meter design and debugging
6. Already hand on the low power and thermal design is a big plus to this job opening

Job Requirements

1. MSEE or equivalent plus 8+ years industry experience required
2. Strong communication skills preferred.
3. Hand-on working experience on the speed binning chip and system testing design

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Job Position

Sr. Design Manager for AVS/controller

Job Location

Austin

Job Description

1. Collaborate with internal cross-functional teams to define and architect AVS and controller for best-in-class SoC power reduction or performance boost solutions for 28nm and 20nm technology nodes and beyond.
2. Drive the circuit, IP, and SoC design, development and deployment of the AVS and controller for a scalable solutions between power and performance.
3. Provide analysis, recommendation and development of autonomous AVS solutions
4. Define power and MHz entitlement direction, execution and achieve next-generation low-power innovations' benefits for Ultra-Low-Voltage (ULV) scaling for voltage-frequency-power entitlement.

Job Requirements

1. MSEE or equivalent with 15+ years of SoC design experience
2. 8+ years of low-power & high-performance technology innovations, SoC design, development, and production experience required.
3. Adaptive Voltage Scaling (AVS) technology and AVS-controller development and production experience is required.
4. Advanced next-generation low-power architecture and development experience is preferred.
5. Significant experience with state-of-the-art power management integration and verification skills is a plus.
6. Strong knowledge with IEEE 1801 is a plus.
7. Strong knowledge of IC front-end design is a plus.

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Job Position

Senior Member of Technical Staff for non-linear SSTA frequency sign-off

Job Location

Austin

Job Description

1. Collaborate with internal cross-functional teams to define and architect DVFS/AVS/Turbo and non-linear SSTA sign-off solution to achieve predictable and deterministic scalable voltage-frequency-power scalable solutions for 28nm and 20nm technology nodes and beyond.
2. Drive the circuit, IP, and SoC design, development and deployment of the DVFS/AVS/Turbo and non-linear SSTA for a scalable solutions across voltage-frequency-power.
3. Provide analysis, recommendation and development of innovative voltage-frequency-power predicable solutions.
4. Define power and MHz entitlement direction, execution and achieve next-generation low-power innovations' benefits for Ultra-Low-Voltage (ULV) scaling for voltage-frequency-power entitlement.

Job Requirements

1. BSEE or equivalent plus 12+ years of IC design experience is required; MSEE or Ph.D. is preferred.
2. 7+ years of low-power & high-performance technology innovations, SoC design, development, and production experience required.
3. Advanced next-generation low-power architecture and development experience and its implication on sign-off is preferred.
4. Significant experience in DVFS/AVS/Turbo sign-off and non-linear SSTA experience required.
5. Significant experience with DVFS/AVS/Turbo/ULV timing closure development and solutions is required.
6. Strong knowledge of C/C++ and/or Java is preferred.

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Job Position

Distinguished Member of Technical Staff for power delivery/switch

Job Location

Austin

Job Description

1. Collaborate with internal cross-functional teams to define and architect power delivery and power switch optimization to achieve scalable voltage-frequency-power scalable solutions for 28nm and 20nm technology nodes and beyond.
2. Drive the circuit, IP, and SoC design, development and deployment of the power delivery and power switch for a scalable solutions across voltage-frequency-power.
3. Provide analysis, recommendation and development of autonomous voltage-frequency-power solutions
4. Define power and MHz entitlement direction, execution and achieve next-generation low-power innovations' benefits for Ultra-Low-Voltage (ULV) scaling for voltage-frequency-power entitlement.

Job Requirements

1. Ph.D. EE or equivalent with 15+ years of industry experience.
2. 9+ years of low-power & high-performance technology innovations, SoC design, development, and production experience required.
3. SoC power delivery and power switch architecture for scalable voltage-frequency-power entitlement and its production experience is required.
4. Scalable power switch architecture for Adaptive Voltage Scaling (AVS) is required.
5. Advanced next-generation low-power architecture and development experience is preferred.
6. Strong knowledge of IEEE 1801 and SoC back-end design experience is preferred.

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Job Position

Distinguished Member of Technical Staff for Design for LV

Job Location

Austin

Job Description

1. Collaborate with internal cross-functional teams to define and architect Design for Low-Voltage strategies and to deliver a voltage-frequency-power scalable solutions for 28nm and 20nm technology nodes and beyond.
2. Drive the circuit, IP, and SoC design, development and deployment of the voltage-frequency-power scalable solutions.
3. Provide analysis, recommendation and development of autonomous voltage-frequency-power solutions
4. Define power and MHz entitlement direction, execution and achieve next-generation low-power innovations' benefits for Ultra-Low-Voltage (ULV) scaling for voltage-frequency-power entitlement.

Job Requirements

1. BSEE or equivalent plus 12+ years industry experience required
2. 8+ years of low-power & high-performance technology innovations, SoC design, development, and production experience required.
3. Design for low-voltage architecture for scalable voltage-frequency-power entitlement and its production experience is required.
4. SoC Adaptive Voltage Scaling (AVS) architecture, and low-voltage transistor-level circuit behavior and effects from manufacturing variation and its impact on yield is required.
5. Advanced next-generation low-power architecture and development experience is preferred.
6. Strong knowledge of low-voltage circuits or analog design experience is preferred.

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Job Position

Sr. Designer for SoC and CPU tech. & implementation (incl spec)

Job Location

Hsin Chu, Taiwan

Job Description

1. SOC integration for internal project from spec to production
2. power network, power switch architecture & implementation
3. low level circuit knowledge, such as power process decision, cell library, low power SRAM
4. low power design, DVFS, AVS, ABB, multi-Vt, MTCMOS, etc
5. Thermal and low power meter design and debugging
6. Already hand on the low power and thermal design is a big plus to this job opening

Job Requirements

1. MSEE or equivalent plus 8+ years industry experience required
2. Strong communication skills preferred.
3. Hand-on working experience on the speed binning chip and system testing design

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Job Position

Sr. Designer for SoC implementation

Job Location

Hsin Chu, Taiwan

Job Description

1. SOC integration for internal project
 2. power switch and architecture design
 3. low level circuit knowledge, such as power process decision, cell library, low power SRAM
 4. low power design, DVFS, AVS, ABB, multi-Vt, MTCMOS, etc
 5. Thermal and low power meter design and debugging
- Already hand on the low power and thermal design is a big plus to this job opening

Job Requirements

Experienced on the speed binning chip and system testing design

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Job Position

Telephony Framework Sr. Designer

Job Location

Taipei, Taiwan

Job Description

1. Responsible for wireless telecom development
2. Responsible for Operator IOT and developing Operator requirements
3. Responsible for improving debugging tool on Android
4. Responsible for enriching Android SDK on Telephony domain
5. Responsible for optimizing Smartphone performance

Job Requirements

Must have:

1. Experience on wireless telecomm protocol stack for 3 years, especial for Non-access Stratum
2. Experience on CMUX/ AT command for 3 years
3. Experience on Android Telephony framework for 2 years
4. Experience on Smartphone development for 5 years

Nice to have:

1. Experience on be an architect for complex SW module
2. Experience on java programming for 5 years
3. Experience on Object oriented programming
4. Experience on Mediatek solution of Smartphone or Feature phone

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Job Position

Browser Sr. Designer

Job Location

Taipei, Taiwan

Job Description

1. Research WebKit engine, platform, and environment
2. Design and develop WebKit features to support new web applications
3. Fine-tune WebKit performance
4. Develop deep expertise in multiple areas including web-based technologies, web monitoring and APIs
5. Play an active role and work with web developers, planner team, and platform services team to implement web applications

Job Requirements

Must have:

1. Familiar with WebKit design and implementation
2. Familiar with XML, HTML 5, JavaScript
3. With more than 3-5 years experience of browser development

Nice to have:

1. With WebKit development experience on Android

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Job Position

Database Sr. Designer

Job Location

Taipei, Taiwan

Job Description

1. Android Database planning, buildups, maintain, monitor, backup recovery, performance tuning, bottleneck finding and data manipulation
2. Review database design and structure
3. Optimize database operations for performance

Job Requirements

1. Familiar with Database related domain knowledge
2. Solid knowledge in computer science fundamentals, including data structures, programming languages, algorithms, software engineering, database theory and operating systems
3. With more than 3-4 years experience of database development
4. Experienced in Java programming

Nice to have:

1. Experienced in linux/android development

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Job Position

Software Management Expert

Job Location

San Jose

Job Description

1. Collaborate with internal cross-functional teams to define software management strategies and to deliver scalable solutions for multi-product, multi-chipset source code management.
2. Drive the design, development and deployment of CI (Continuous Integration) solutions.
3. Provide analysis and recommendation on overall performance of the software management eco-system.
4. Define/refine the security model and policies for both internal and external access to our code base.

Job Requirements

1. Bachelors degree in Computer Science or related field
2. Extensive knowledge and experience with popular scripting languages: python, perl, make, etc.
3. More than 10 years direct experience with a proven track record.
4. Significant experience with popular SCM, such as Performance and GIT.
5. Significant experience with developing and integrating Continuous Integration solutions.
6. Familiarity and experience with Linux and/or Android operating systems is a plus.
7. Strong knowledge of C/C++ and/or Java is preferred.

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Job Position

Security Architect

Job Location

San Jose

Job Description

1. Collaborate with product marketing and cross-functional teams to define security requirements and guide the development of advanced security solutions to enable DRM, trusted executions, secure contents/transactions, mobile banking/ payments, and many other secure applications in mobile phones.
2. Conduct systems security and vulnerability analyses.
3. Promote security-aware software platform development, from design to implementation with a goal to improve the robustness of system security controls.
4. Make recommendations on system security architecture in relation to hardware and software structures based on ARM TrustZone enabling technology and GlobalPlatform Trusted Execution Environment (TEE) framework.
5. Involve in the development of secure boot / secure download process with the development teams.
6. Drive the software security roadmaps & strategies for Smartphone products.

Job Requirements

1. Master above degree in Computer Science or related field
2. Strong knowledge of C/C++ and/or Java
3. Significant experience developing embedded software, and in particular multi-threaded software
4. Strong knowledge with Linux, Android or other embedded OS
5. Strong knowledge of the ARM architecture
6. 10+ years of relevant industrial experience in software security architecture and application developments.
7. Solid hands-on experience in modern DRM and cryptography implementations.
8. Proven experience in ARM TrustZone base system design and development required.
9. Familiarity and experience with Linux and/or Android operating systems, and their security features.
10. Strong knowledge of content protection methods on mobile platforms.
11. Familiarity with the industry's security requirements on mobile platforms.

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Job Position

NFC System Sr. Designer

Job Location

Hsin Chu, Taiwan

Job Description

1. NFC system architecture development.
2. NFC controller IC development.

Job Requirements

1. Minimum 2+ years of NFC experience
2. Experience with RFID/NFC controller IC development.
3. Proficiency with RFID/NFC standards (NFC Forum standards, ISO, ETSI, and ECMA)
4. Familiar with system design (such as R/W, P2P, and card mode), CLF RF design (such as powered by the field), CLF BB design (such as highly integrated architecture design for NFC-A/B/F/V), CPU design (such as low MIPS and low power CPU), coprocessor design (such as RNG, timer, and AES/DES)
5. Familiar with SE design (optional) is a plus.

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Job Position

NFC Middleware Sr. Designer

Job Location

Hsin Chu, Taiwan

Job Description

1. NFC software architecture design and development
2. NFC ecosystem, application, and standard analysis

Job Requirements

1. Minimum 2+ years of NFC experience
2. Experience with NFC software/middleware development.
3. Familiar with NFC software/middleware architecture and protocol stack
4. Proficiency with NFC related standards such as NFC Forum Type 1 ~ 4 Tag, LLCP, NDEF, RTD, proprietary Tag specifications, EMVCo specification, JSR 257, JSR 177, HCI, SWP, ISO 7816, etc.
5. Familiar with NFC ecosystem and application.
6. Familiar with Android NFC software architecture is a plus